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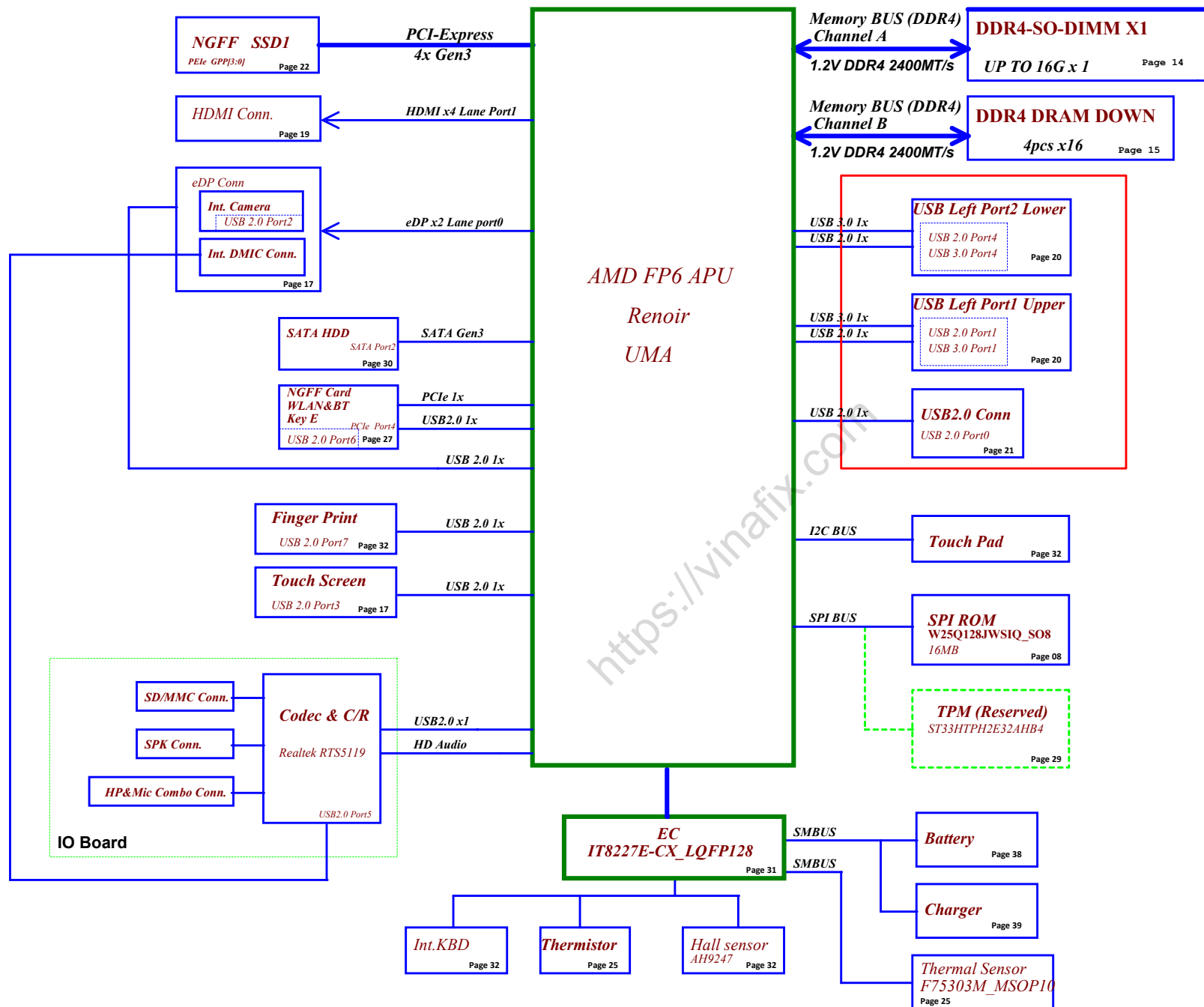
S350 Renoir M/B Schematics Document

AMD FP6 Renoir with DDR4

2020-01-06

REV: 1.0

Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		Cover Page	
2019/02/27		2020/02/27			
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Voltage Rails (O --> Means ON , X --> Means OFF)

State \ power plane	B+ (+20VSB) +3VL +5VLP	+5VALW +3VALW (+3VALW_APU) +1.8VALW +0.75VALW	+2.5V +1.2V	+5VS +3VS +1.8VS +0.75VS +0.6VS +VDDC_VDD +VDDCR_SOC
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	GPU	BATT	IT8227	SODIMM	WLAN	Thermal Sensor	APU	Charger	PMIC
EC_SMB_CK1 EC_SMB_DA1	IT8227 +3VL	X	V		X	X	X	X	V	X
EC_SMB_CK2 EC_SMB_DA2	IT8227 +3VS	X	X		X	X	V +3VS	V SIC/SID	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8227 +3VL	X	X		X	X	X	X	X	V
APU_SCLK0 APU_SDATA0	APU	X	X	X	X	X	X		X	X

	SOURCE	Device
TP_I2C3_SCL TP_I2C3_SDA	APU +3VALW	Touch Pad +3VS

APU I2C address

Device	Address
Elan: SA469D-22HA 69x104x1.0	?
Synaptics: TM-P3255-008 69x104x1.0	?

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

Port List

HSIO Port	Device
GFX	N/A
GPP	SSD
	WLAN
	N/A
	HDD
	N/A
USB3.0	N/A
	USB 3.0 Port1 Upper
	USB 3.0 Port2 Lower
	N/A
USB2.0	USB2.0
	USB 3.0 Port1 Upper
	Camera
	Touch Screen
	USB 3.0 Lower
	Cardreader
	BT
	Finger Print

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
ME@	Connector
EMC@	EMC Part
EMC NS@	EMC reserve Part
RF@	RF Part
TPM@	TPM part
HDT@	HDT Debug part
REDRV@	Redriver part
17@	17' HDD Redriver part
NO17@	17' HDD Redriver reserve part
TS@	Touch Screen Part
NOTS@	Touch Screen reserve Part
FP@	Finger print Part
NOFP@	Finger print reserve Part

EC SM Bus0 address

Device	Address
PD	
PMIC	0X34

EC SM Bus1 address

Device	Address
Charger	0b00010010
Battery	?

EC SM Bus2 address

Device	Address
APU SB-TSI	relate to F3x1E4[SbiAddr] or Address Select Pins setting
Thermal Sensor	10011011b(read) 10011010b(write)

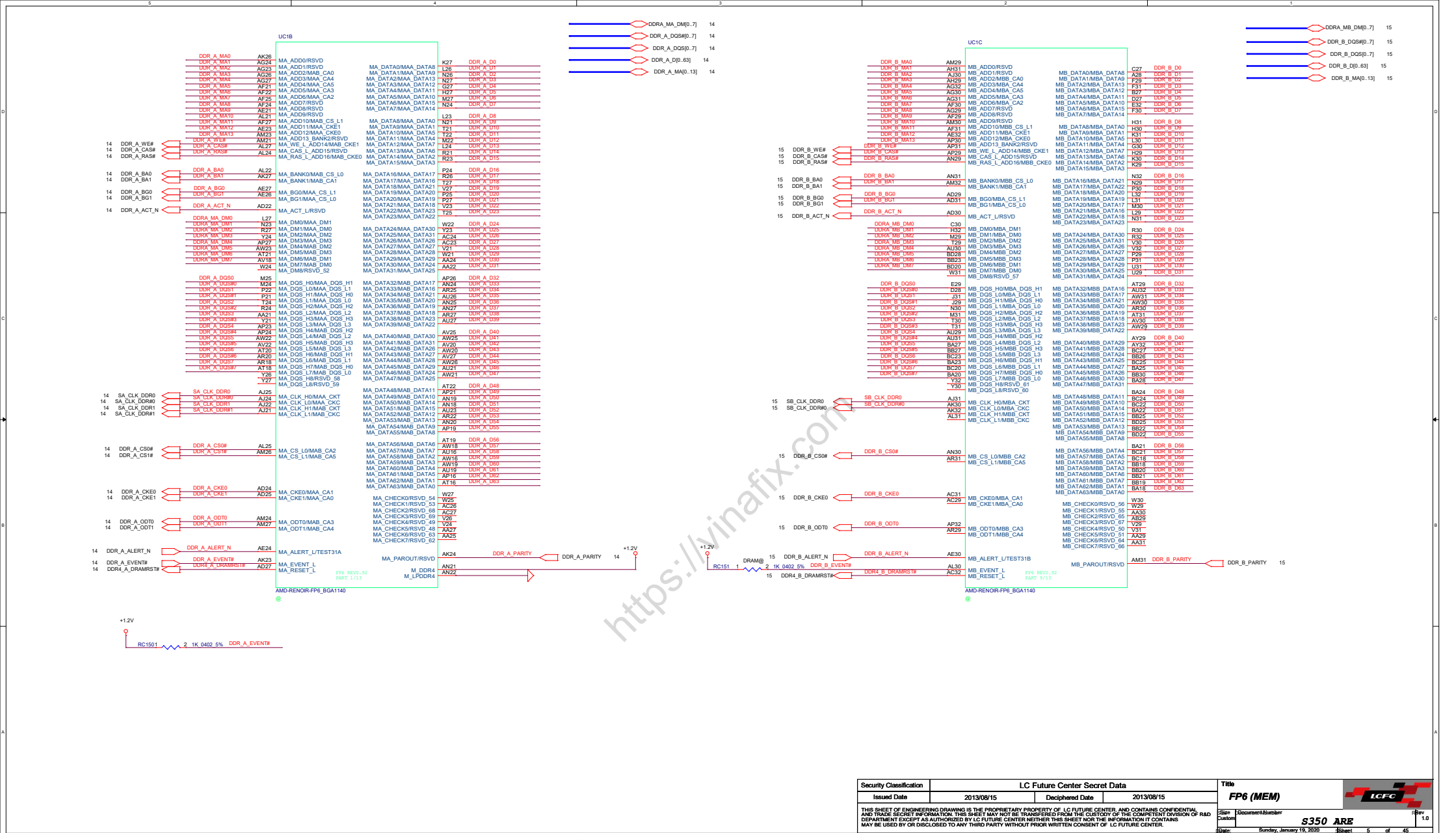
EC SM Bus3 address


Device	Address
Expand IT8013	0100,A2,A1,A0

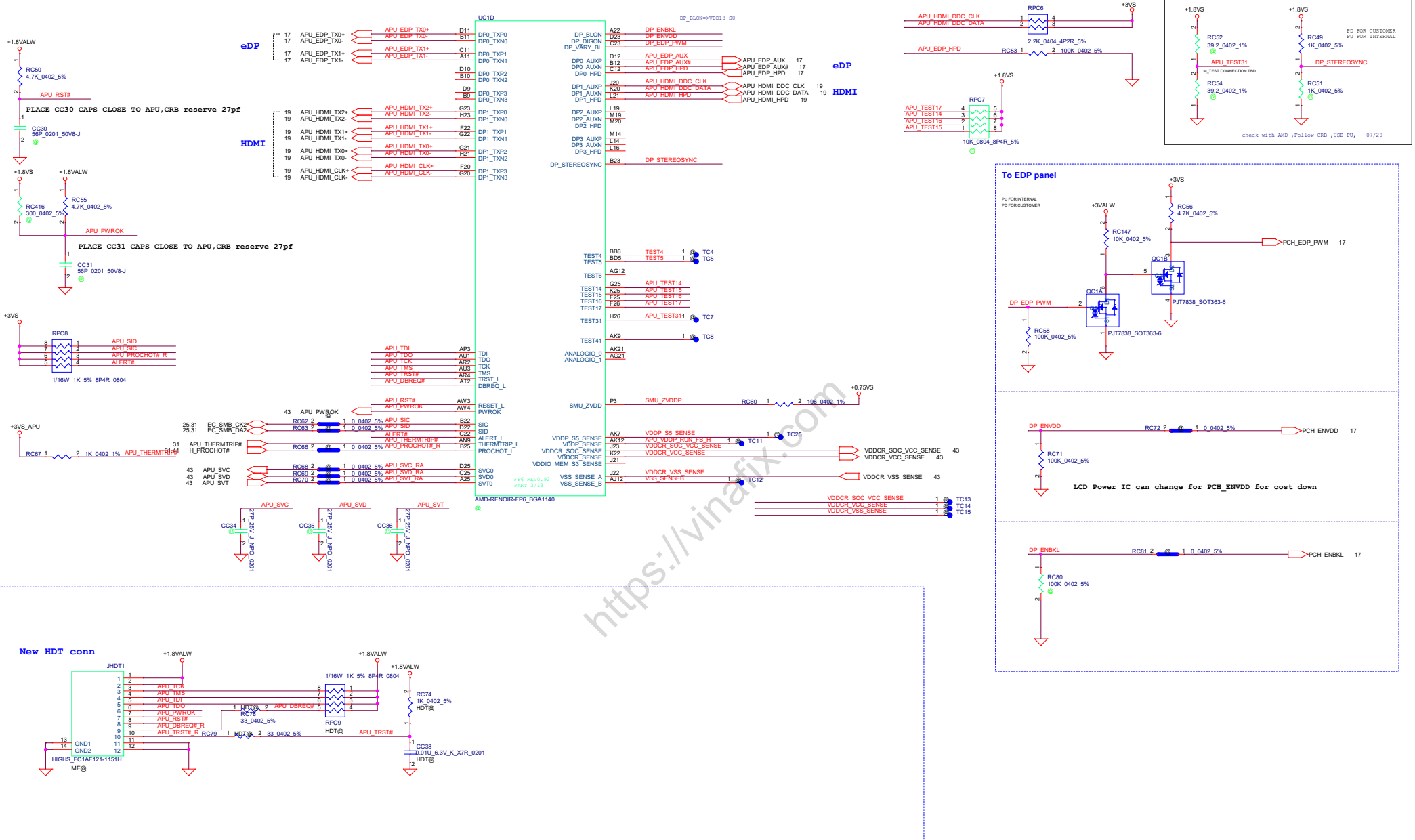
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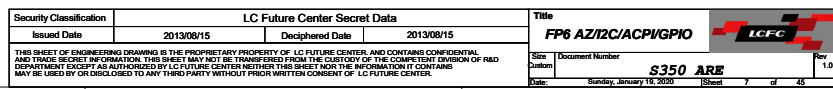


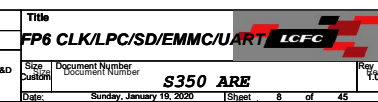
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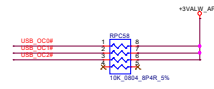
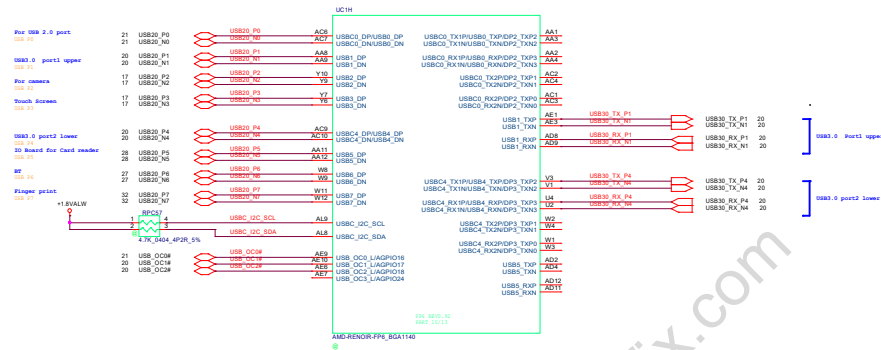
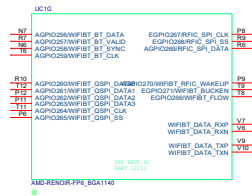


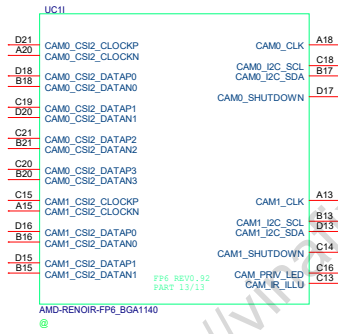
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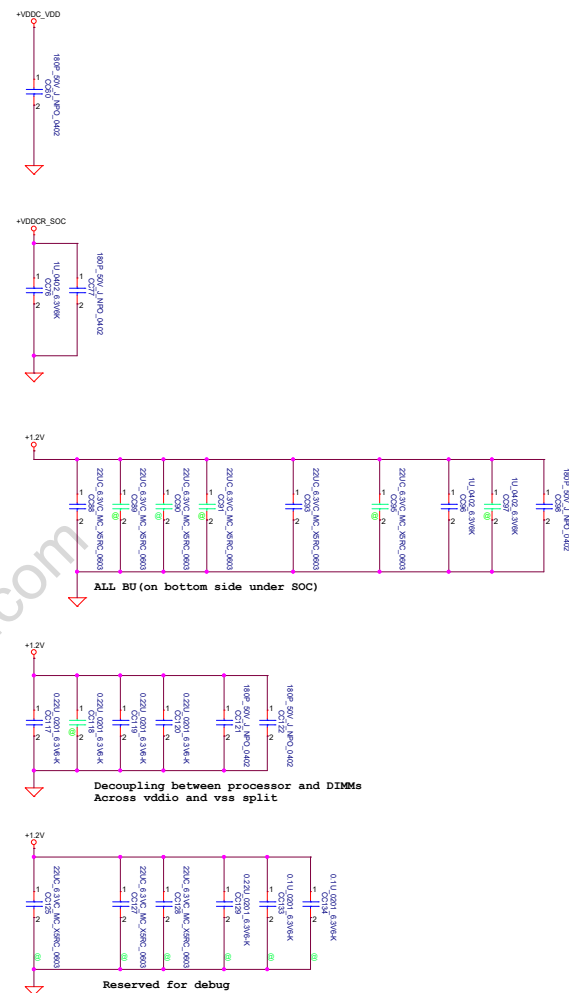


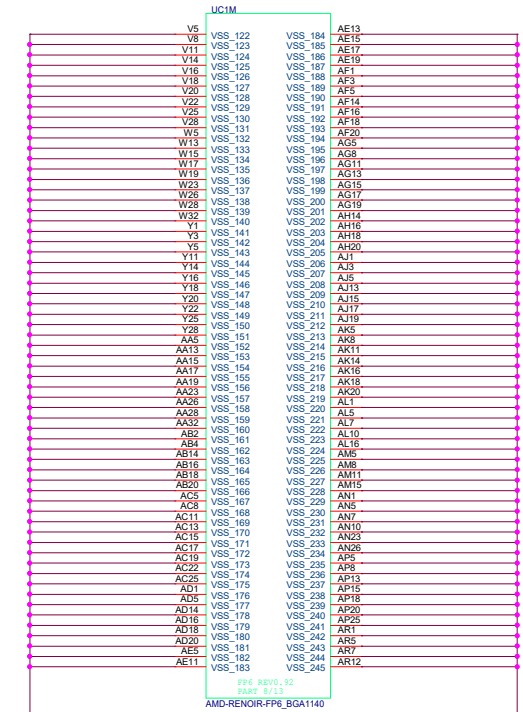
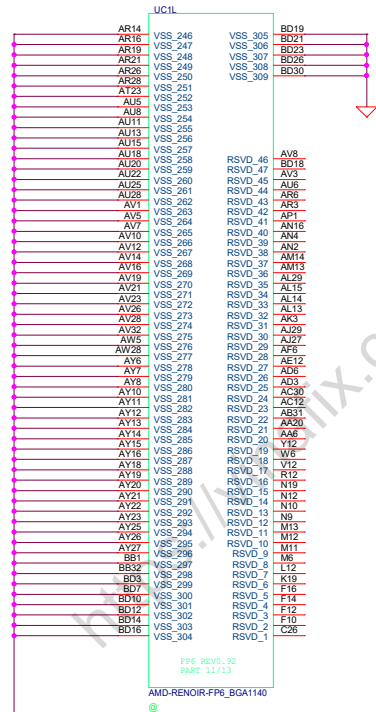
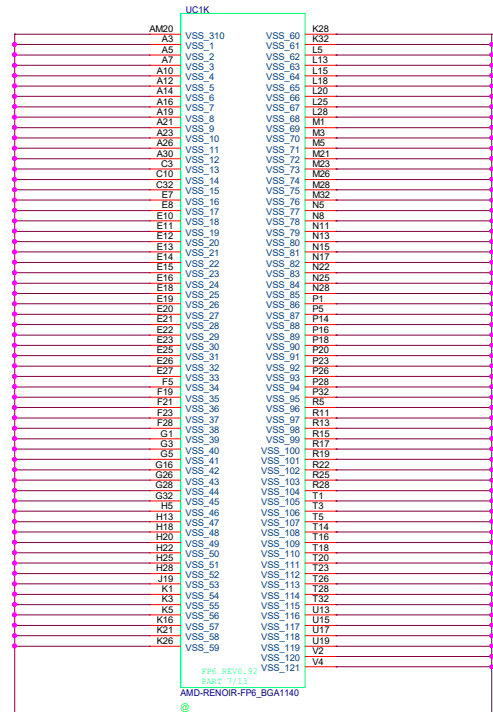


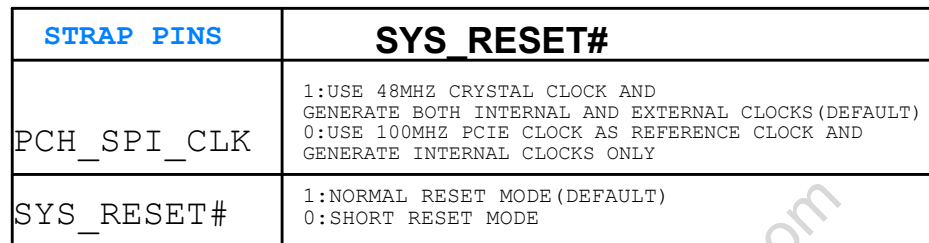
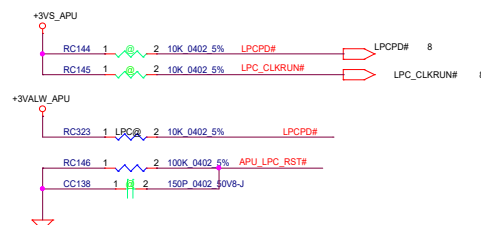









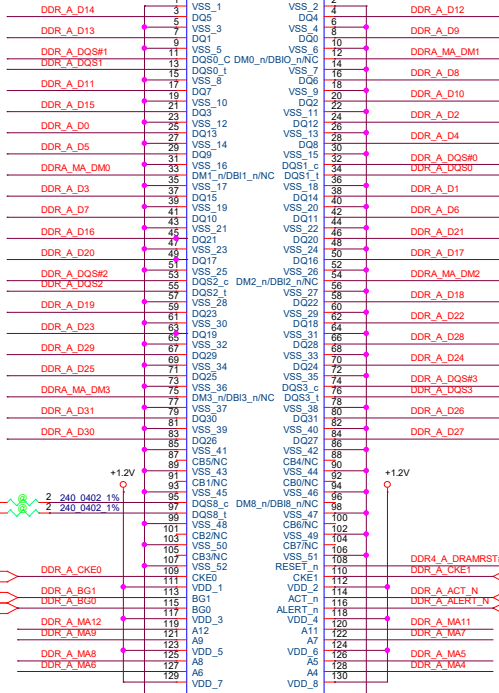


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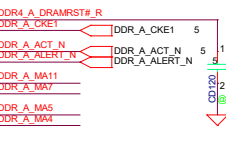
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update JDDR1 symbol 1129

JDDR1A

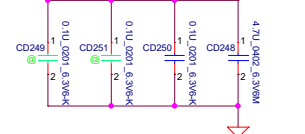


for MEM_MB_RST# overshoot issue

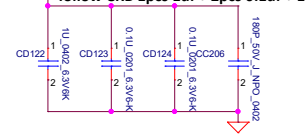


Layout Note: Place near JDDR1

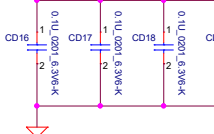
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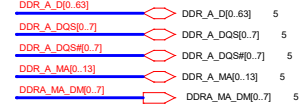
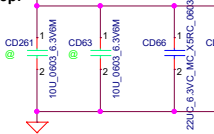
follow CRB 1pcs 1uf + 2pcs 0.1uf + 1pcs 180pf



follow CRB 6pcs 0.1uf



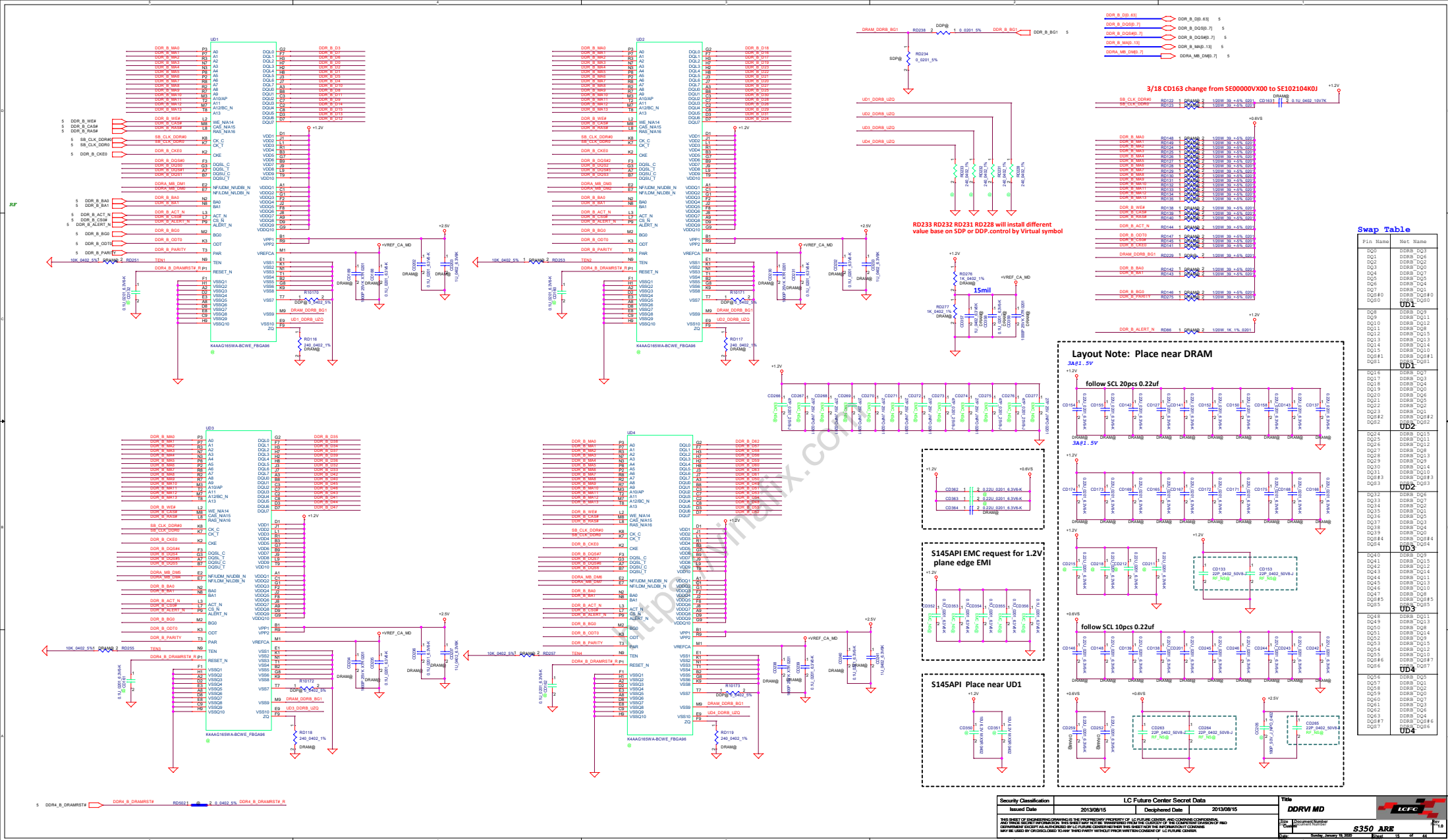
follow CRB 1pcs 1uf + 2pcs 0.1uf + 1pcs 180pf



Swap Table

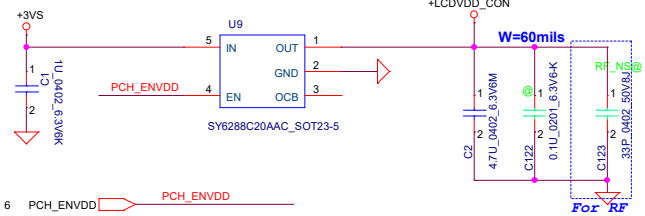
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DQ2	DDR_A_DQ2
DQ3	DDR_A_DQ3
DQ4	DDR_A_DQ4
DQ5	DDR_A_DQ0
DQ6	DDR_A_DQ1
DQ7	DDR_A_DQ7
DQS#0	DDR_A_DQS#0
DQ13	DDR_A_DQ8
DQ8	DDR_A_DQ13
DQ9	DDR_A_DQ9
DQ10	DDR_A_DQ14
DQ11	DDR_A_DQ10
DQ12	DDR_A_DQ12
DQ13	DDR_A_DQ8
DQ14	DDR_A_DQ15
DQ15	DDR_A_DQ11
DQS#1	DDR_A_DQS#1
DQ51	DDR_A_DQ51
DQ16	DDR_A_DQ20
DQ17	DDR_A_DQ21
DQ18	DDR_A_DQ22
DQ19	DDR_A_DQ19
DQ20	DDR_A_DQ16
DQ21	DDR_A_DQ17
DQ22	DDR_A_DQ23
DQ23	DDR_A_DQ18
DQS#2	DDR_A_DQS#2
DQ52	DDR_A_DQ52
DQ24	DDR_A_DQ28
DQ25	DDR_A_DQ29
DQ26	DDR_A_DQ31
DQ27	DDR_A_DQ27
DQ28	DDR_A_DQ24
DQ29	DDR_A_DQ25
DQ30	DDR_A_DQ30
DQ31	DDR_A_DQ26
DQS#3	DDR_A_DQS#3
DQ53	DDR_A_DQ53
DQ32	DDR_A_DQ33
DQ33	DDR_A_DQ37
DQ34	DDR_A_DQ34
DQ35	DDR_A_DQ38
DQ36	DDR_A_DQ32
DQ37	DDR_A_DQ36
DQ38	DDR_A_DQ35
DQ39	DDR_A_DQ39
DQS#4	DDR_A_DQS#4
DQ54	DDR_A_DQ54
DQ40	DDR_A_DQ44
DQ41	DDR_A_DQ40
DQ42	DDR_A_DQ47
DQ43	DDR_A_DQ43
DQ44	DDR_A_DQ41
DQ45	DDR_A_DQ45
DQ46	DDR_A_DQ46
DQ47	DDR_A_DQ42
DQS#5	DDR_A_DQS#5
DQ55	DDR_A_DQ55
DQ48	DDR_A_DQ48
DQ49	DDR_A_DQ49
DQ50	DDR_A_DQ55
DQ51	DDR_A_DQ50
DQ52	DDR_A_DQ52
DQ53	DDR_A_DQ53
DQ54	DDR_A_DQ54
DQ55	DDR_A_DQ51
DQS#6	DDR_A_DQS#6
DQ56	DDR_A_DQ56
DQ57	DDR_A_DQ56
DQ58	DDR_A_DQ63
DQ59	DDR_A_DQ59
DQ60	DDR_A_DQ60
DQ61	DDR_A_DQ57
DQ62	DDR_A_DQ58
DQ63	DDR_A_DQ62
DQS#7	DDR_A_DQS#7
DQ57	DDR_A_DQ57

SPD Address = A0H

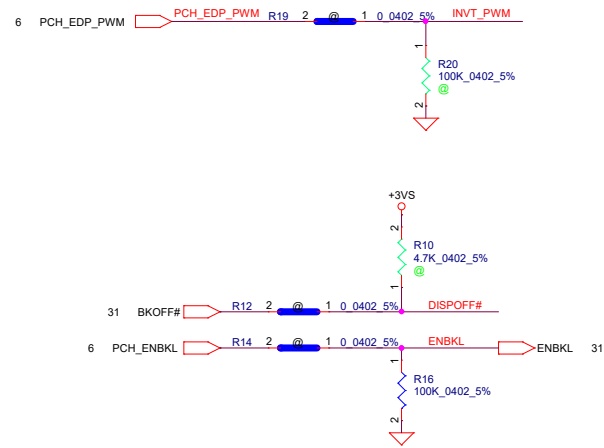


5					4					3					2					1				
D																								
C																								
B																								
A																								
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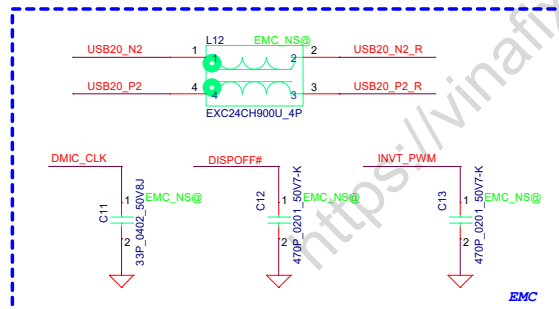
LCD POWER CIRCUIT



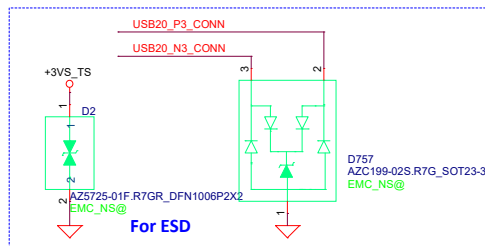
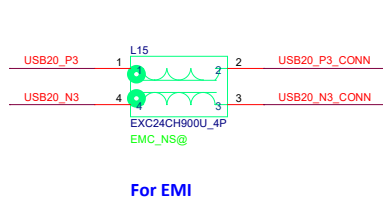
APU output enable Voh min is 1.8V-0.45V=1.35V



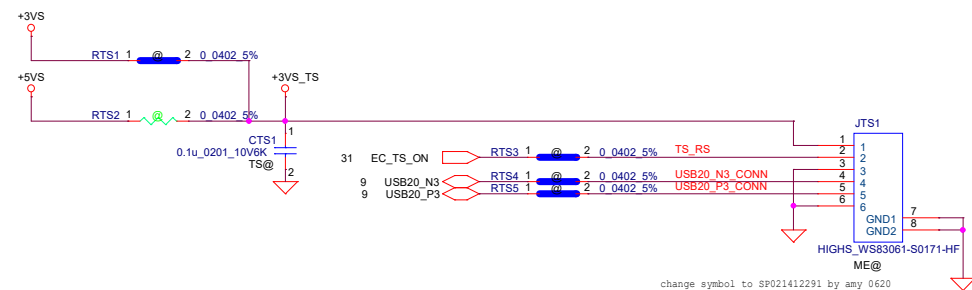
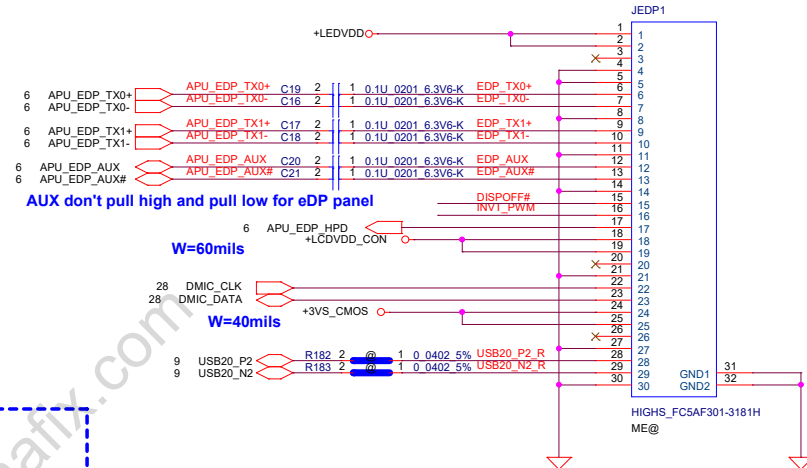
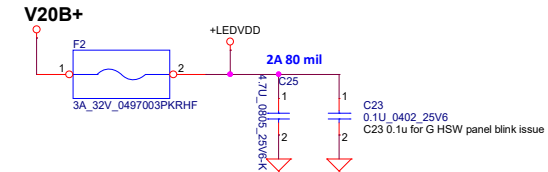
CMOS Camera



Touch Screen




B+ to +LEDVDD POWER

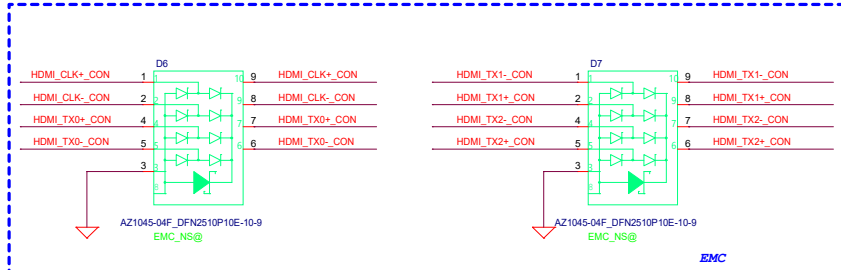
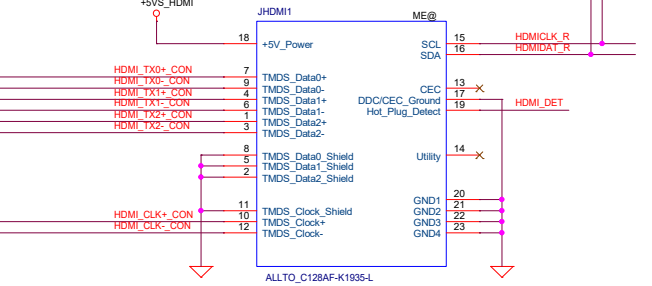
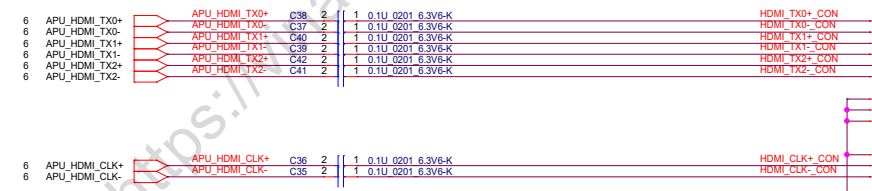
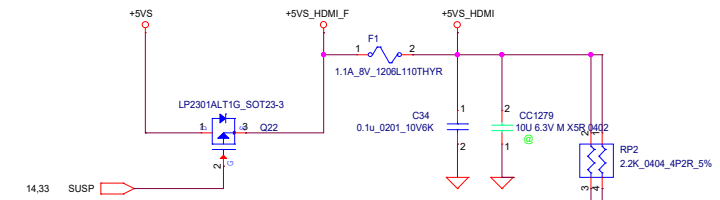
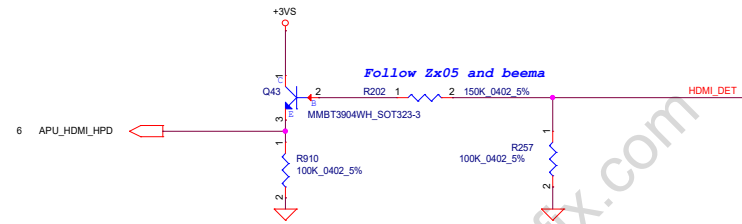
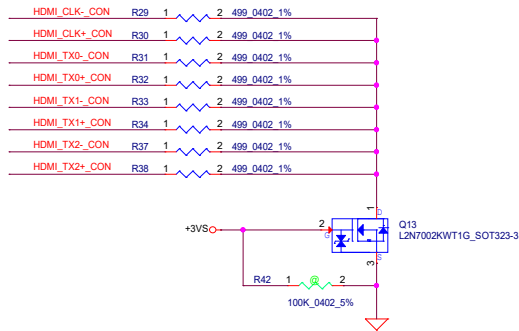
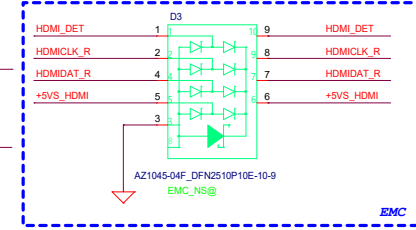
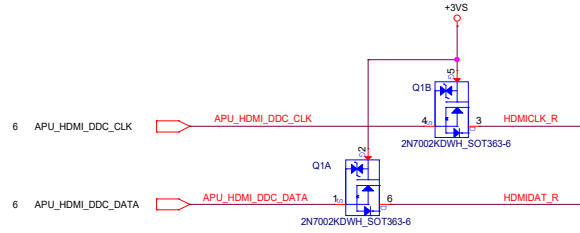
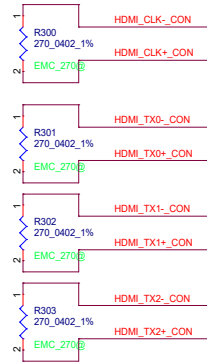



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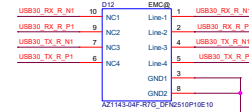
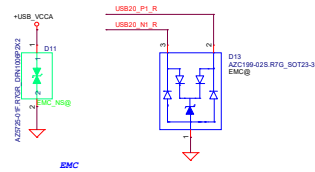
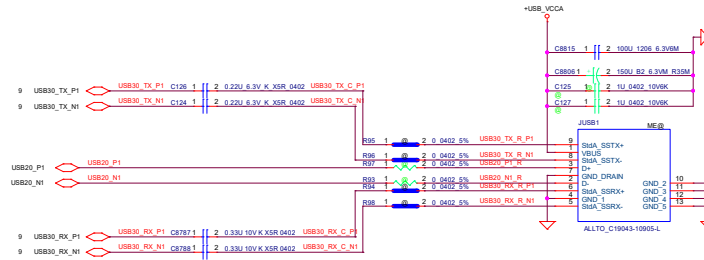
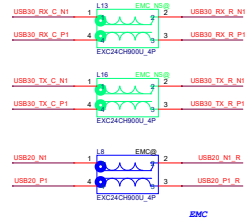
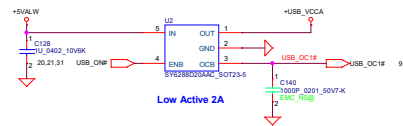
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7/29 S145API EMC request for HDMI

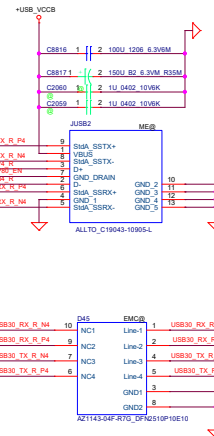
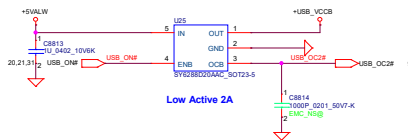
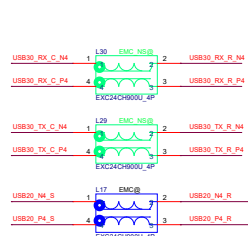


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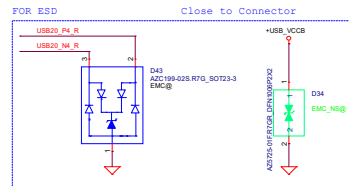
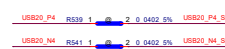
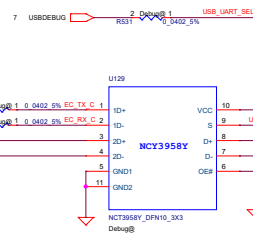
LEFT SIDE USB3.0 PORT x2



USB3.0 PORT



For USB Debug Function

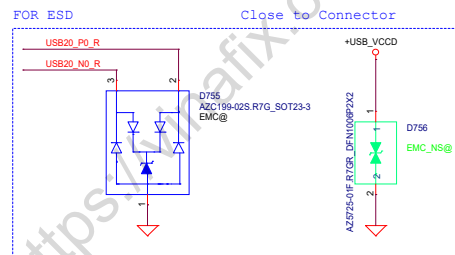
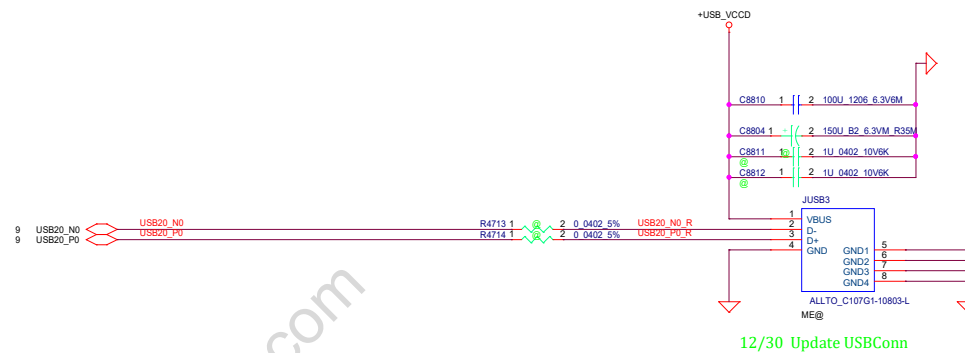


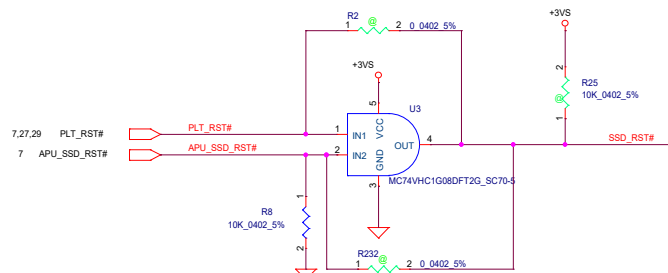
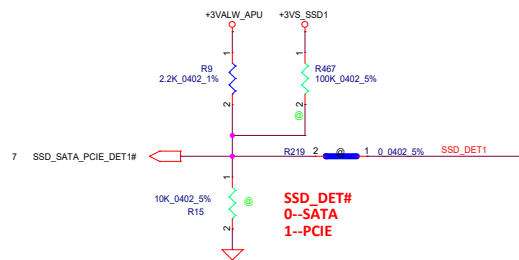
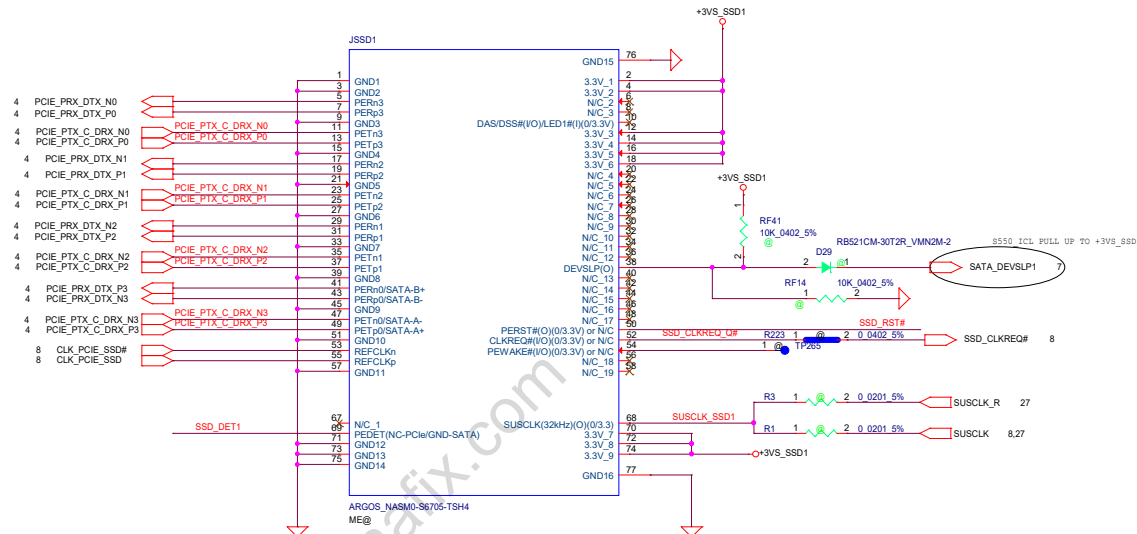
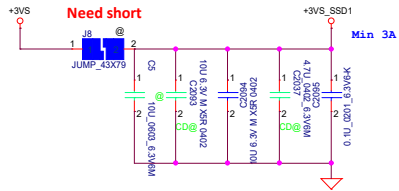
USBDEBUG	Kernel debug
Set Input	Set Input
Set Output Low	ENABLER

UART_P80_EN	POST 80
Set Input	ENABLER
Set Output Low	ENABLER

DE#	S	FUNCTION
0	0	ENABLER
1	0	ENABLER
2	0	ENABLER

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Issued Date	Deciphered Date	2017/08/15
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Size	Document Number	Rev
3530	ARE	1.0
Issue	Revision	20 of 44

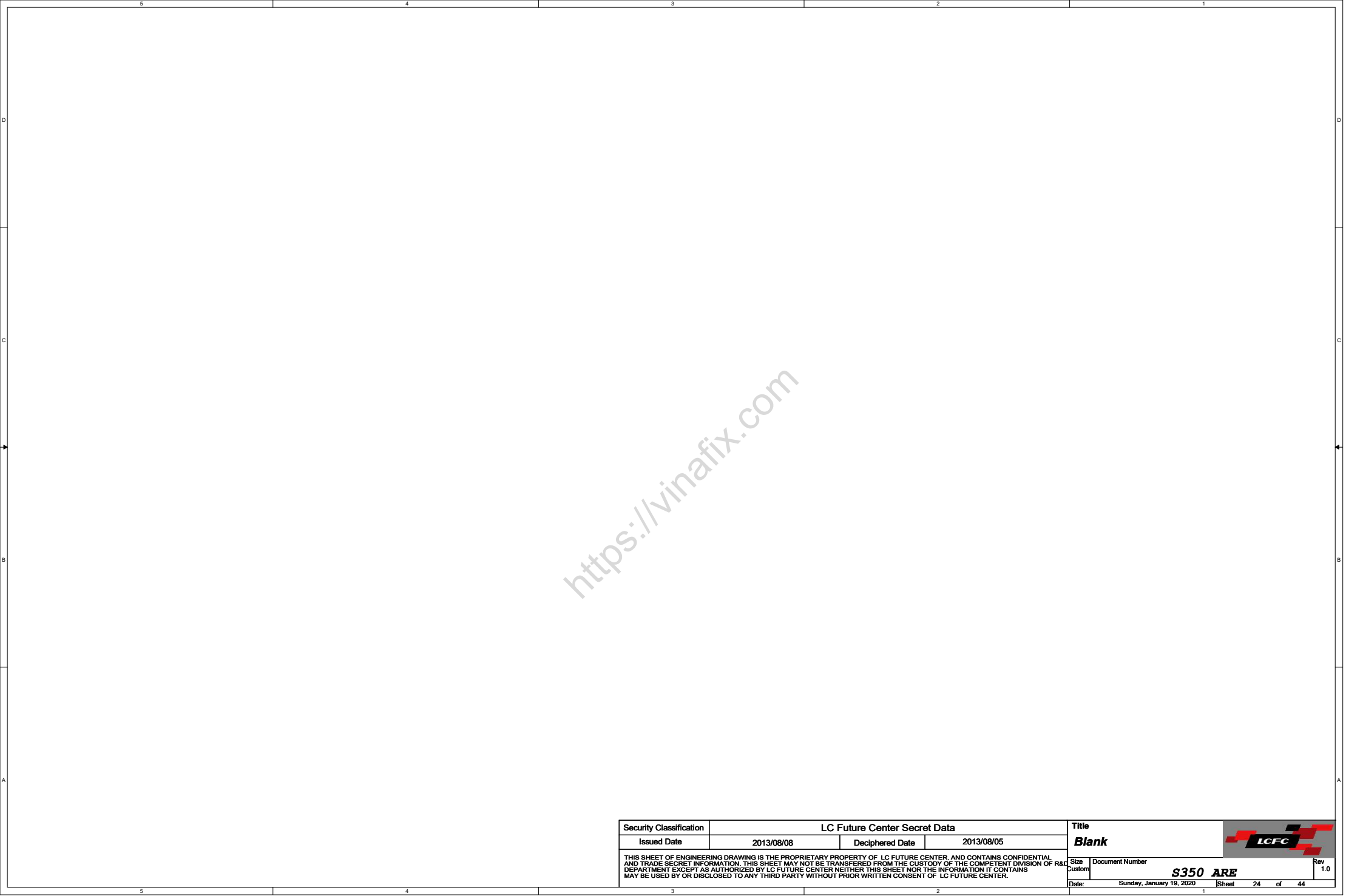




AND Gate:

PLT_RST#	APU_SSD_RST#	SSD_RST#
L	L	L
L	H	L
H	L	L
H	H	H

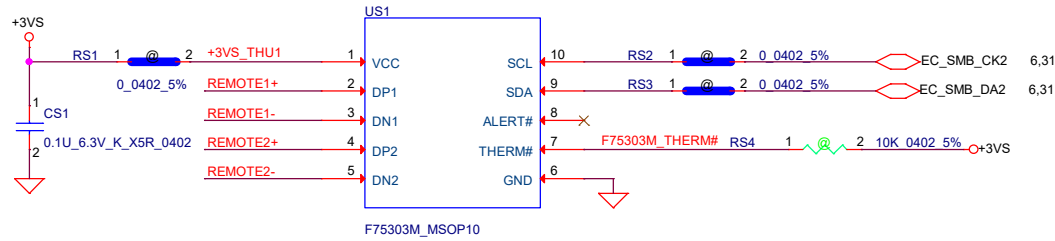
5		4		3		2		1	
D									
C									
B									
A									



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Issued Date	2013/08/08	Deciphered Date	2013/08/05
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Title			
Blank			
Size	Document Number		Rev
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Thermal Sensor placed nearby SO-DIMM

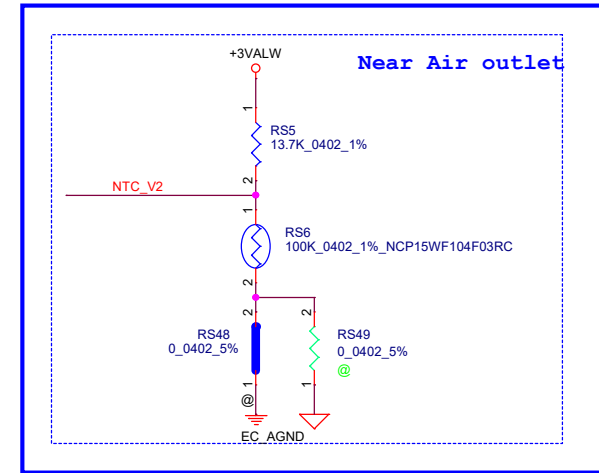


Address 1001_101xb

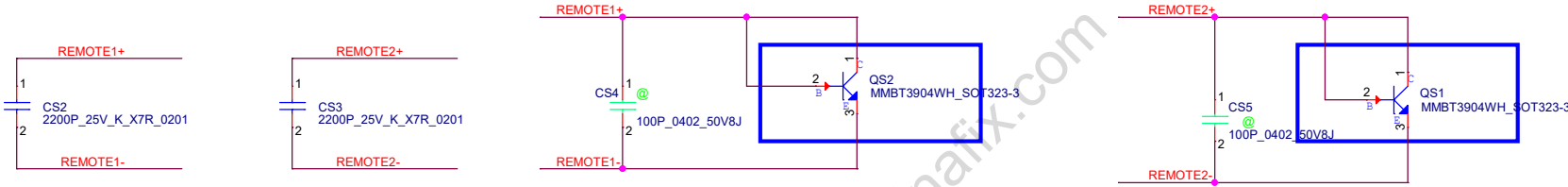
Internal pull up 1.2K to 1.5V

R for initial thermal shutdown temp

REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

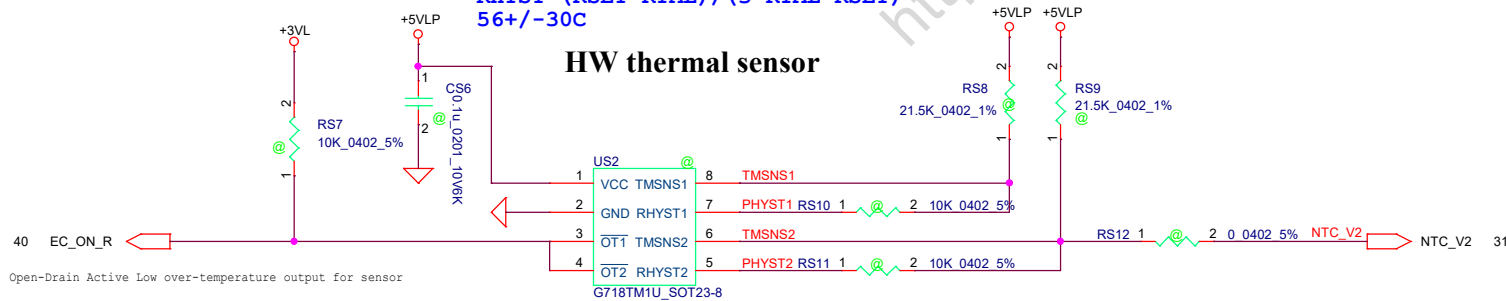


Close APU



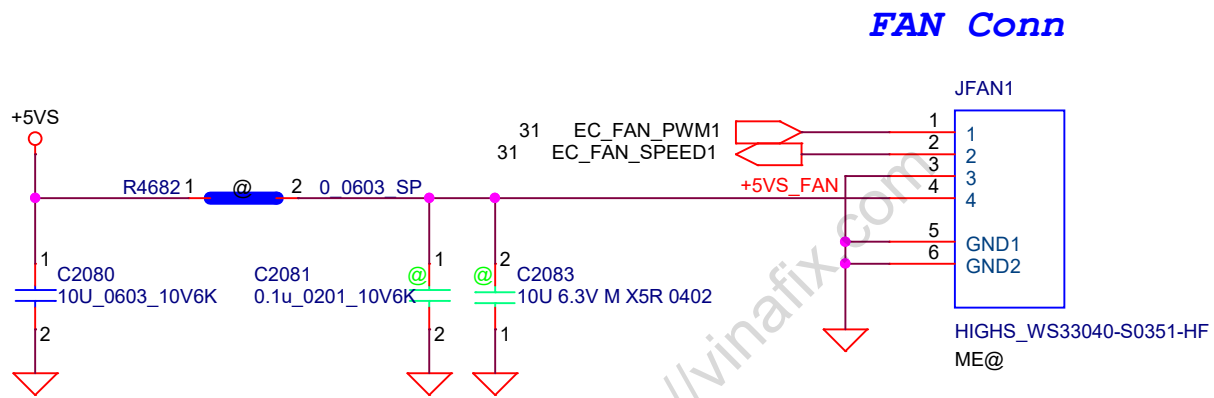
over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML) / (3*RTML-RSET)
56+/-30C


HW thermal sensor



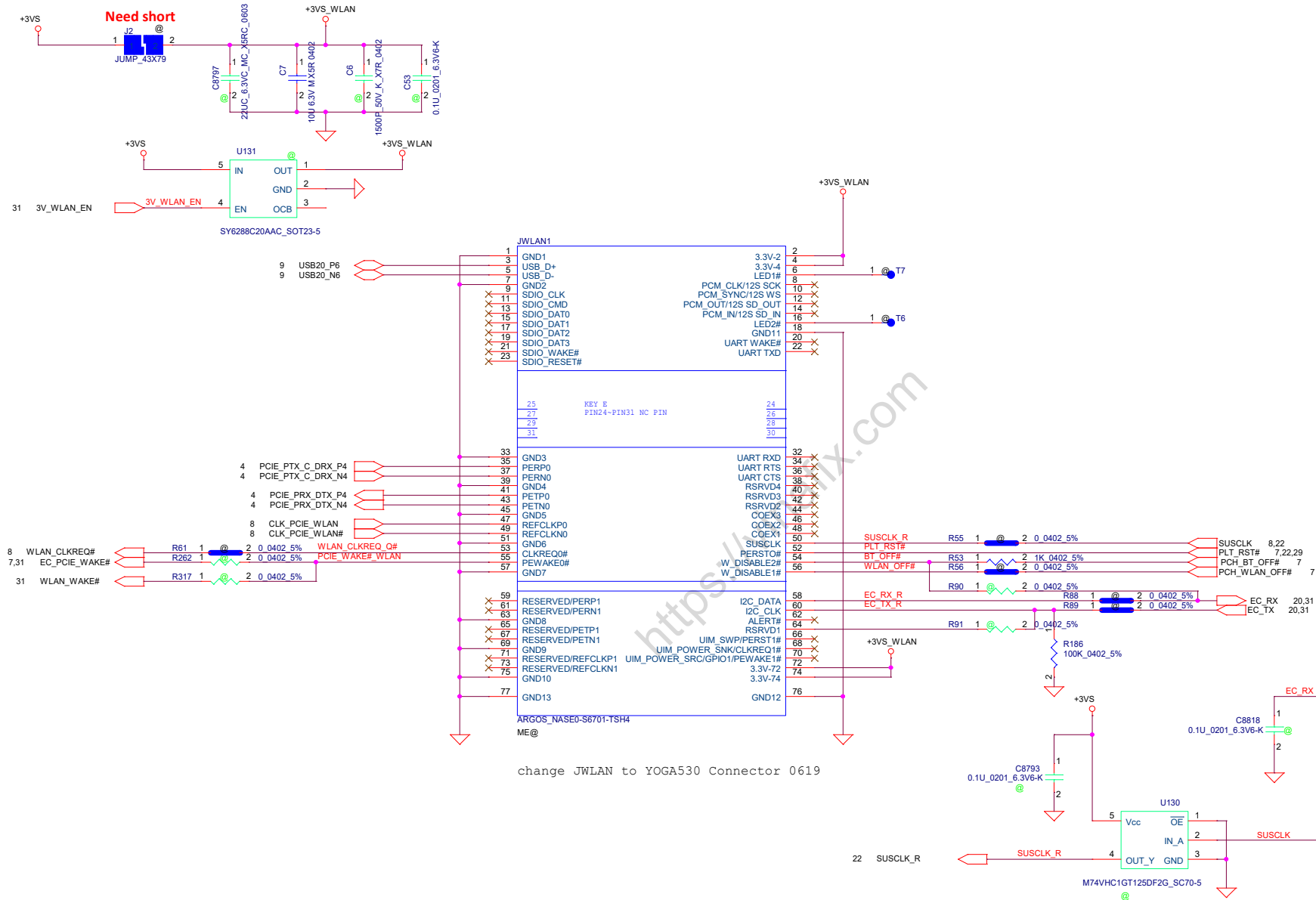
Open-Drain Active Low over-temperature output for sensor

Security Classification	LC Future Center Secret Data		Title	THERMAL SENSOR	
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						Date:	Sunday, January 19, 2020		Sheet	26 of 44

Mini-Express Card(WLAN/WiMAX)

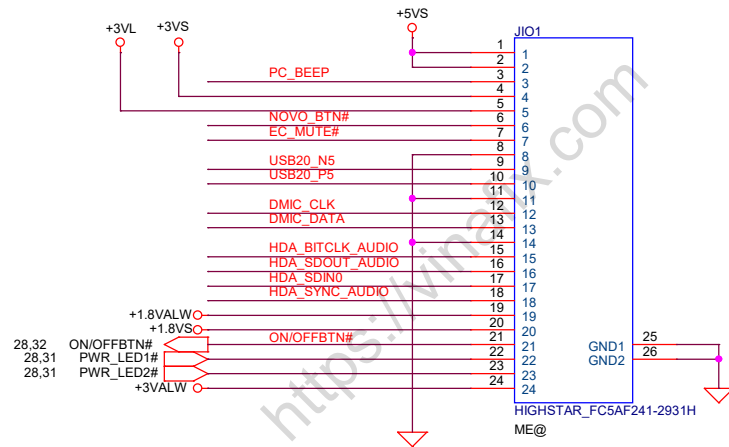
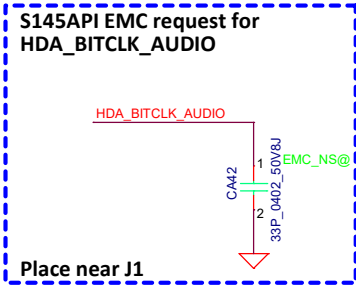
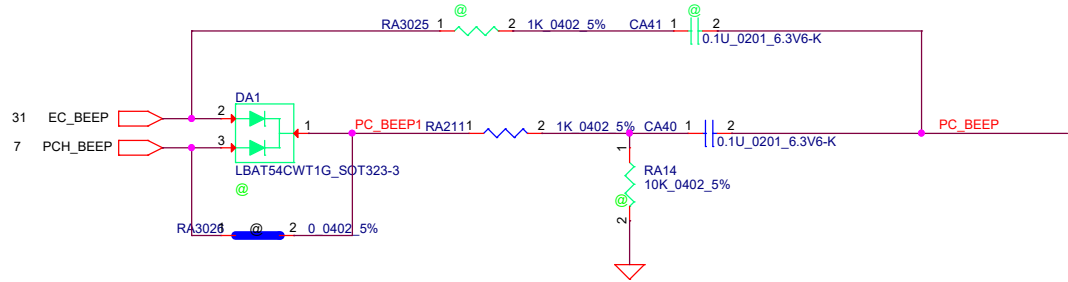


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Issued Date	2013/08/08	Deciphered Date	2013/08/05
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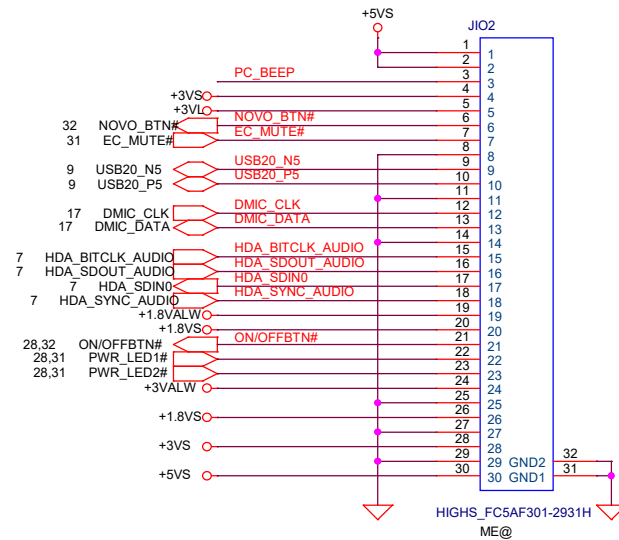
Title		 	
Size	Document Number	Rev	
Custom	S350 ARE	1.0	
Date:	Sunday, January 19, 2020	Sheet	27 of 44




IO Connector

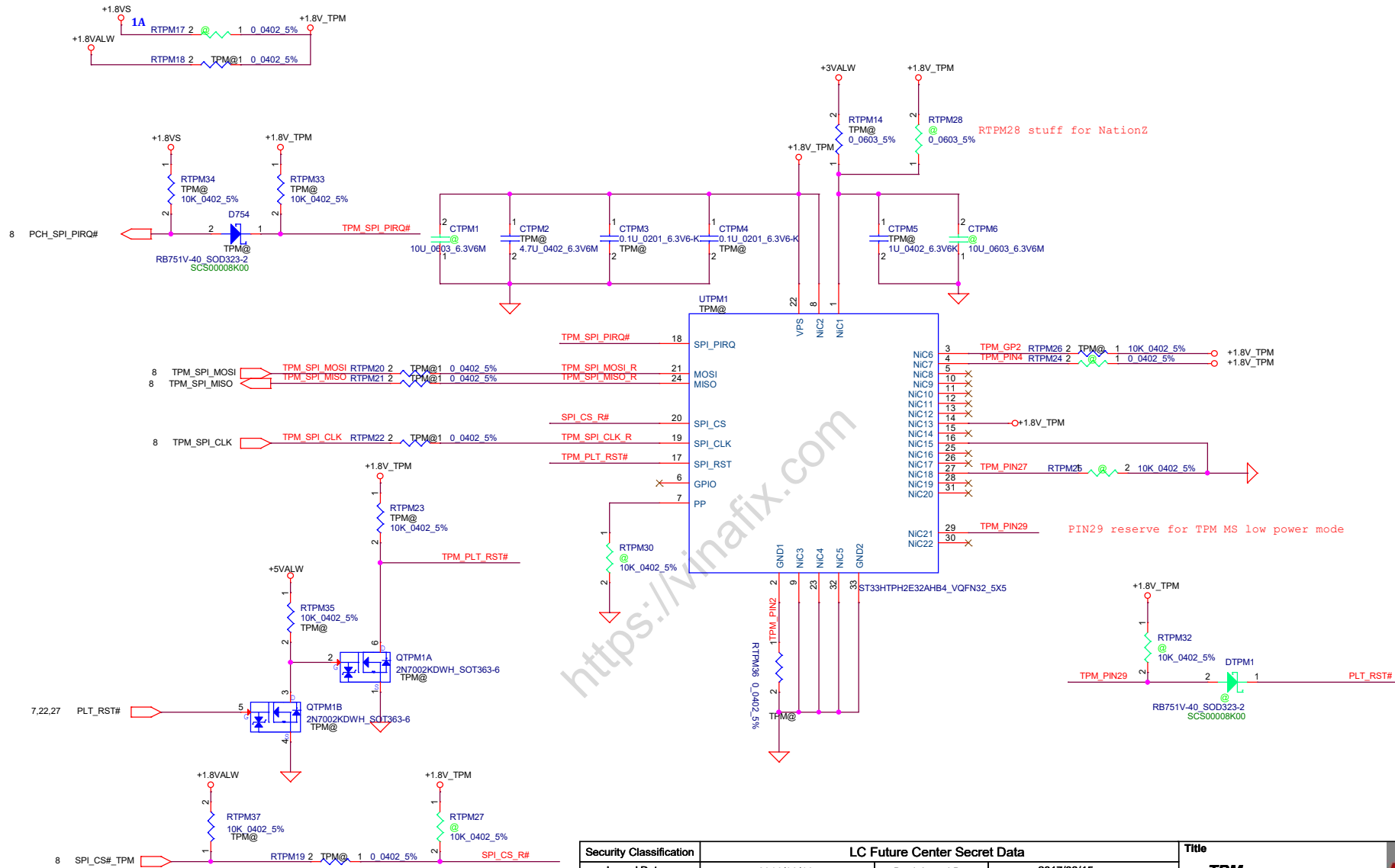



24Pin CONN



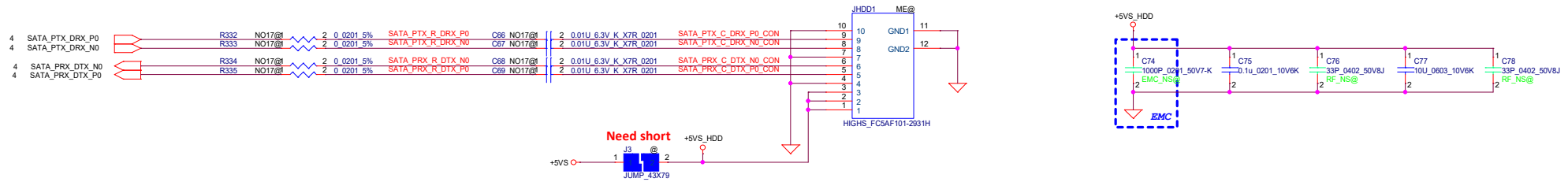
30Pin CONN

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Size		Document Number		S350 ARE				Rev 1.0	
Date:		Sunday, January 19, 2020				Sheet 28 of 44			

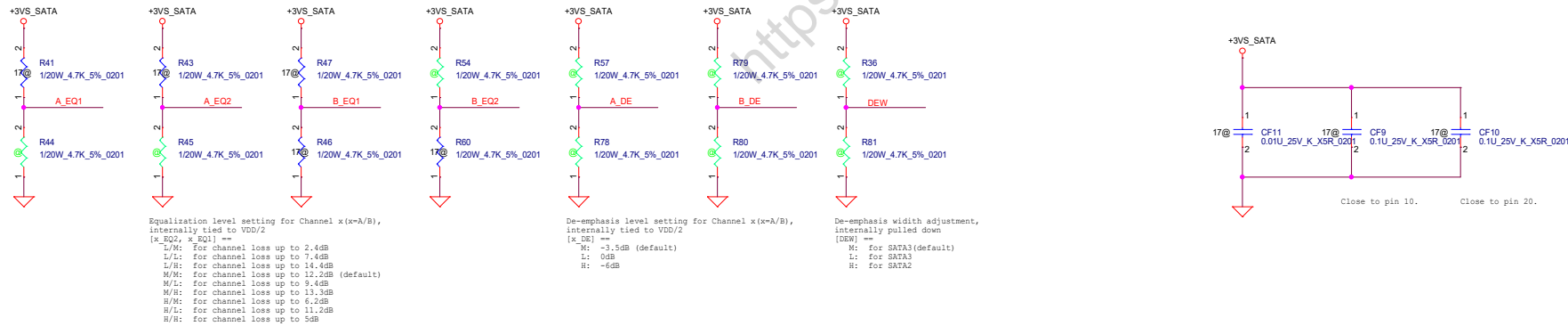
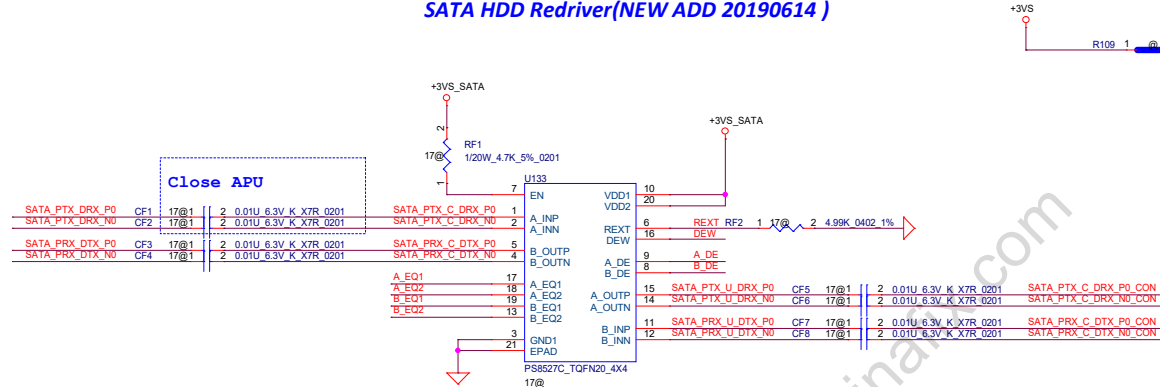


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Issued Date		2016/08/16		Deciphered Date		2017/08/15				TPM					
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										Date: Sunday, January 18, 2020		Sheet: 29 of 44			


SATA HDD Conn.

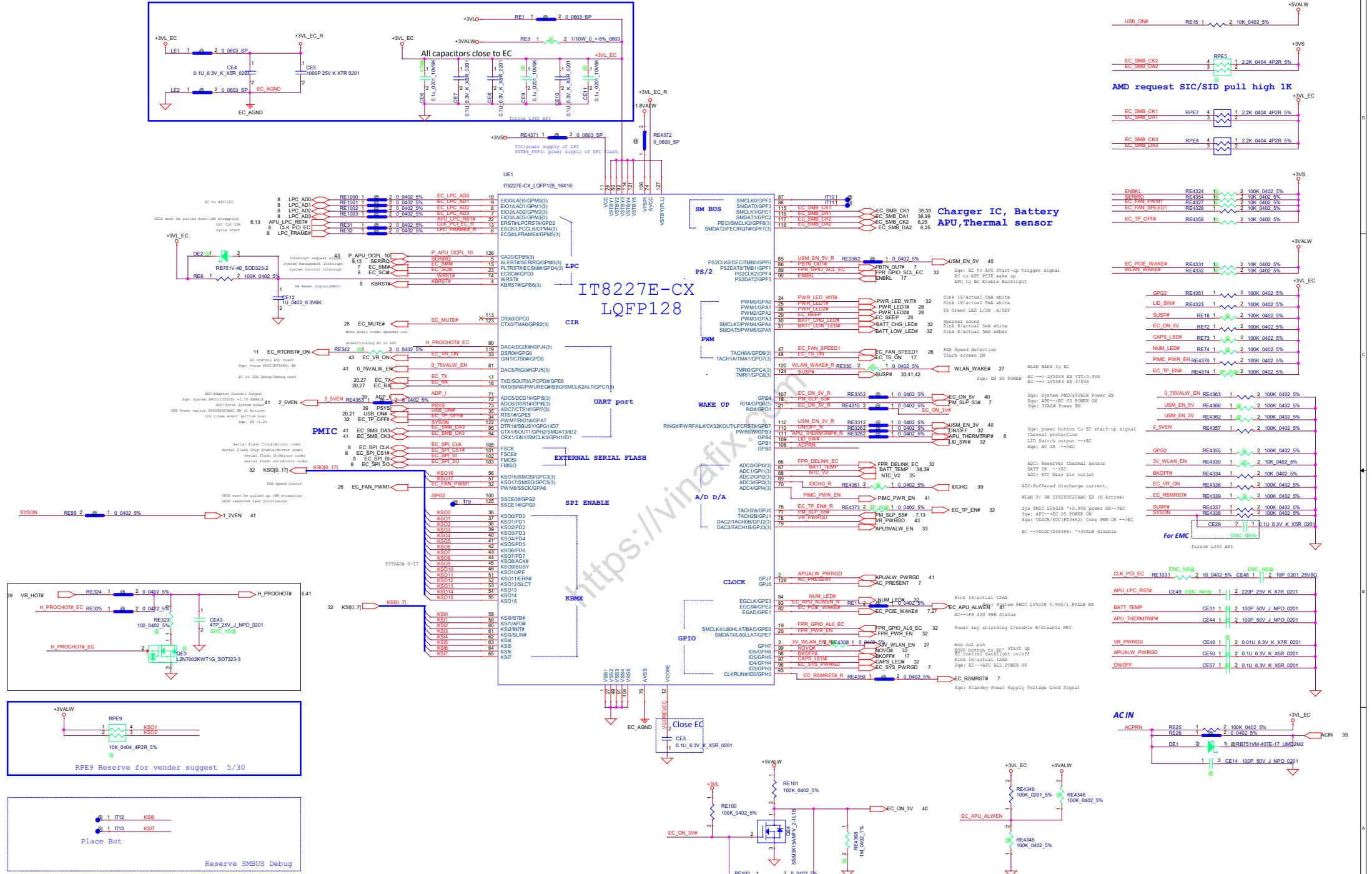


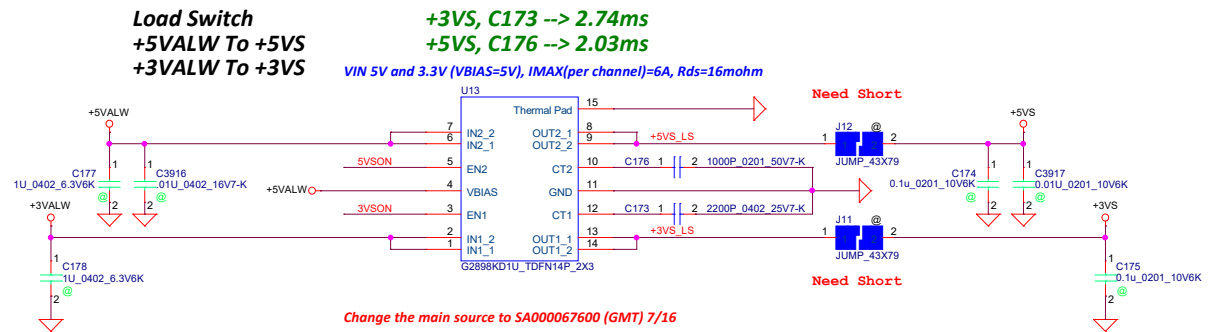
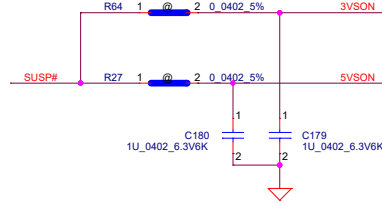
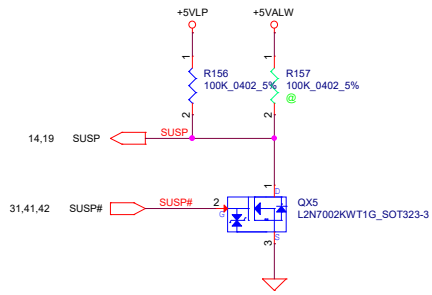
SATA HDD Redriver(NEW ADD 20190614)



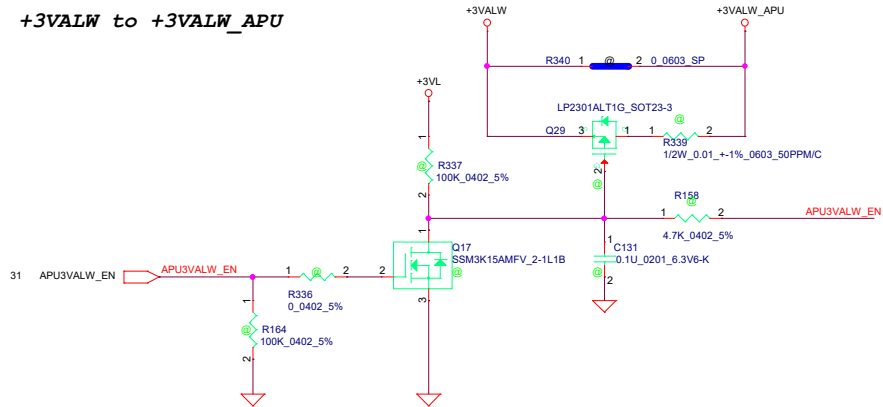
Follow Vendor suggest

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				Date: Sunday, January 19, 2020 Sheet 30 of 44

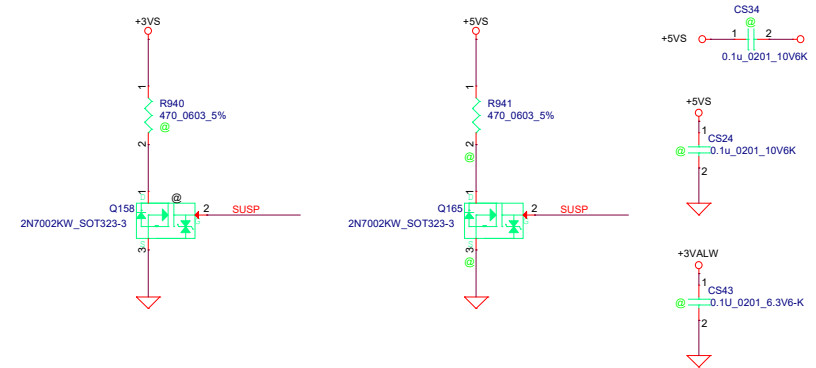




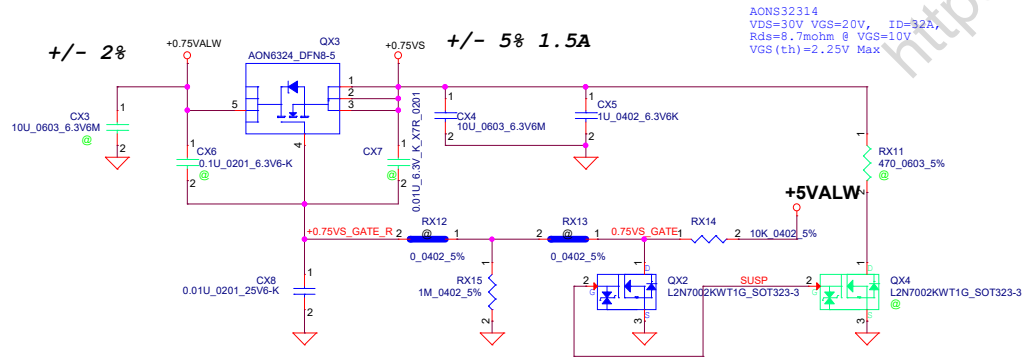
+3VALW to +3VALW_APU



For DisCharge



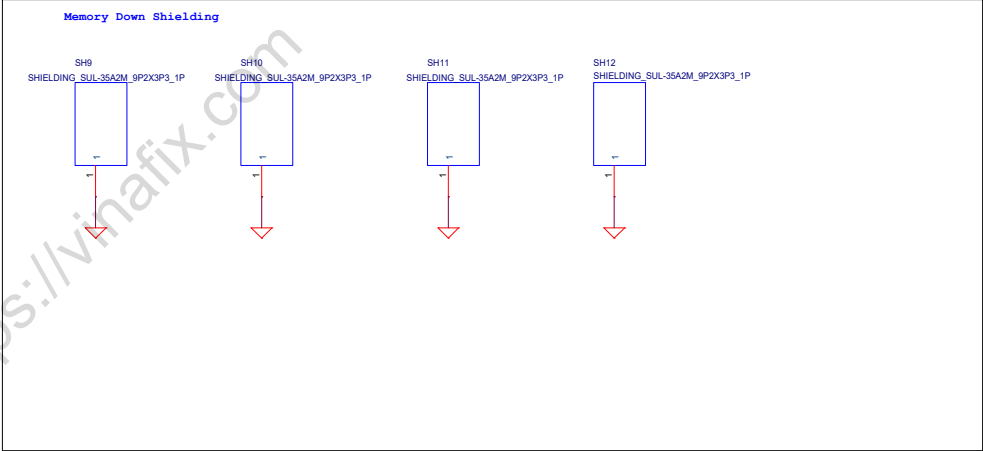
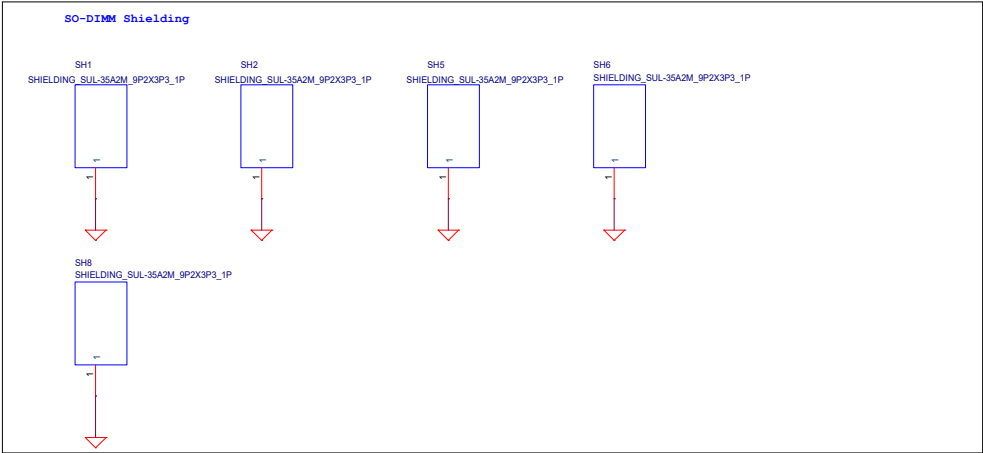
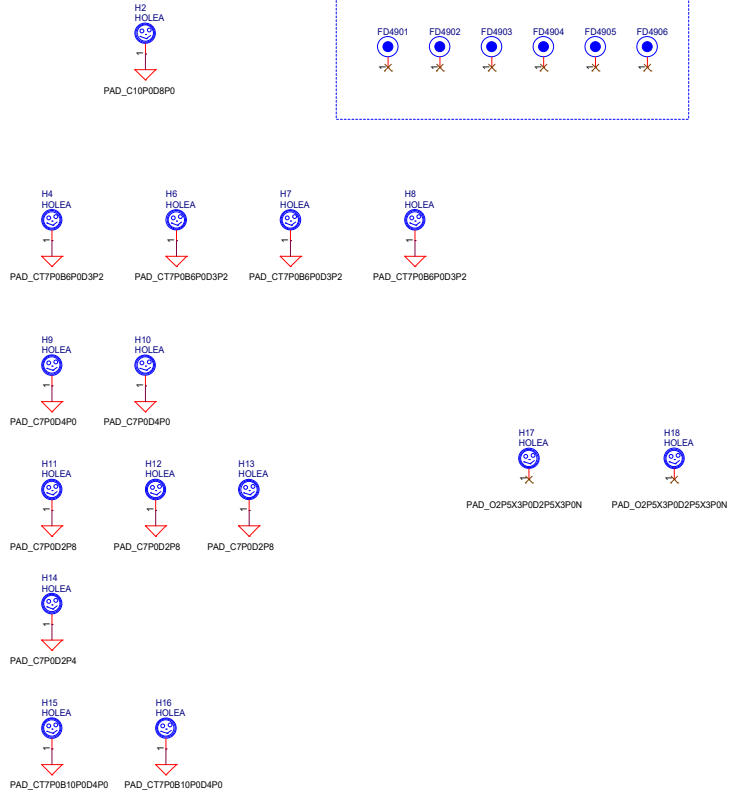
+/- 2%



AON832314
V_{DS}=30V V_{GS}=20V, I_D=32A,
R_{ds}=8.7mohm @ V_{GS}=10V
V_{GS}(th)=2.25V Max

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Title		DC V TO VS INTERFACE	
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Rev		1.0	

Hole



RC35 14MB@
2K 0402 5%
SD0281002B7
N

RC36 14MB@
2K 0402 5%
SD0281002B7
N

14' Mainboard

UC1
RYZEN 7 100-000000083-00 2G
R7@
SA0000AHU20
N

UC1
4700U

UC1
RYZEN 5 100-000000084-00 2.375G
R5@
SA0000AHQ20
N

UC1
4500U

UC1
RYZEN 3 100-000000085-00 2.7G
R3@
SA0000AHW20
N

4300U

check ok
APU type

RC35 15MB@
2K 0402 5%
SD0281002B7
N

RC43 15MB@
10K 0402 5%
SD0281002B7
N

15' Mainboard

ZZZ9 DRAM_S4G@
Samsung
X7649312001
N

ZZZ1 DRAM_M4G@
Micron
X7649312002
N

ZZZ7 DRAM_H4G@
Hynix
X7649412001
N

check ok
DRAM X76 BOM

RC42 17MB@
10K 0402 5%
SD0281002B7
N

RC38 17MB@
2K 0402 5%
SD0281002B7
N

check ok
17' Mainboard

UD1 MD_H8Gb@
H5AN8G6NCJR-XNC
SA0000AC710
N

UD2 MD_H8Gb@
H5AN8G6NCJR-XNC
SA0000AC710
N

UD3 MD_H8Gb@
H5AN8G6NCJR-XNC
SA0000AC710
N

UD4 MD_H8Gb@
H5AN8G6NCJR-XNC
SA0000AC710
N

memory particles

RC44 MD_H8Gb@
10K 0402 5%
SD0281002B7
N

RC41 MD_H8Gb@
2K 0402 5%
SD0281002B7
N

RC45 MD_H8Gb@
10K 0402 5%
SD0281002B7
N

RC46 MD_H8Gb@
2K 0402 5%
SD0281002B7
N

matched resistance

DRAM_Hynix 4G

check ok

UD1 MD_M8Gb@
MT40AS12M16TB-062E-J
SA00009R510
N

UD2 MD_M8Gb@
MT40AS12M16TB-062E-J
SA00009R510
N

UD3 MD_M8Gb@
MT40AS12M16TB-062E-J
SA00009R510
N

UD4 MD_M8Gb@
MT40AS12M16TB-062E-J
SA00009R510
N

memory particles

RC44 MD_M8Gb@
10K 0402 5%
SD0281002B7
N

RC41 MD_M8Gb@
2K 0402 5%
SD0281002B7
N

RC45 MD_M8Gb@
10K 0402 5%
SD0281002B7
N

RC39 MD_M8Gb@
10K 0402 5%
SD0281002B7
N

matched resistance

DRAM_Micron 4G

check ok

RC44 DIMM_ONLY@
10K 0402 5%
SD0281002B7
N

RC41 DIMM_ONLY@
2K 0402 5%
SD0281002B7
N

RC38 DIMM_ONLY@
10K 0402 5%
SD0281002B7
N

RC46 DIMM_ONLY@
2K 0402 5%
SD0281002B7
N

DIMM ONLY

check ok

UD1 MD_S8Gb@
K4AAG16SWC-BCWE
SA0000AC810
N

UD2 MD_S8Gb@
K4AAG16SWC-BCWE
SA0000AC810
N

UD3 MD_S8Gb@
K4AAG16SWC-BCWE
SA0000AC810
N

UD4 MD_S8Gb@
K4AAG16SWC-BCWE
SA0000AC810
N

memory particles

RC44 MD_S8Gb@
10K 0402 5%
SD0281002B7
N

RC41 MD_S8Gb@
2K 0402 5%
SD0281002B7
N

RC38 MD_S8Gb@
10K 0402 5%
SD0281002B7
N

RC39 MD_S8Gb@
10K 0402 5%
SD0281002B7
N

matched resistance

DRAM_Samsung 4G

check ok

PRTC1 RTC@
BATT CR2032 3V 220MAH
X7647H12001
N

RTC

GS451 DA21J200100
GS551 DA21J200100
GS751 DA21J200100

ZZZ13 PCB PN
DA21J200100
N

PCB_MB

check ok

ZZZ14 HDMI@
HDMI PN
RC00000040J
N

HDMI

RD233 SDP@
0_0402_5%
SD0280000B7
N

RD232 SDP@
0_0402_5%
SD0280000B7
N

RD231 SDP@
0_0402_5%
SD0280000B7
N

RD228 SDP@
0_0402_5%
SD0280000B7
N

SDP

RD233 DDP@
240_0402_1%
SD0000097B7
N

RD232 DDP@
240_0402_1%
SD0000097B7
N


RD231 DDP@
240_0402_1%
SD0000097B7
N

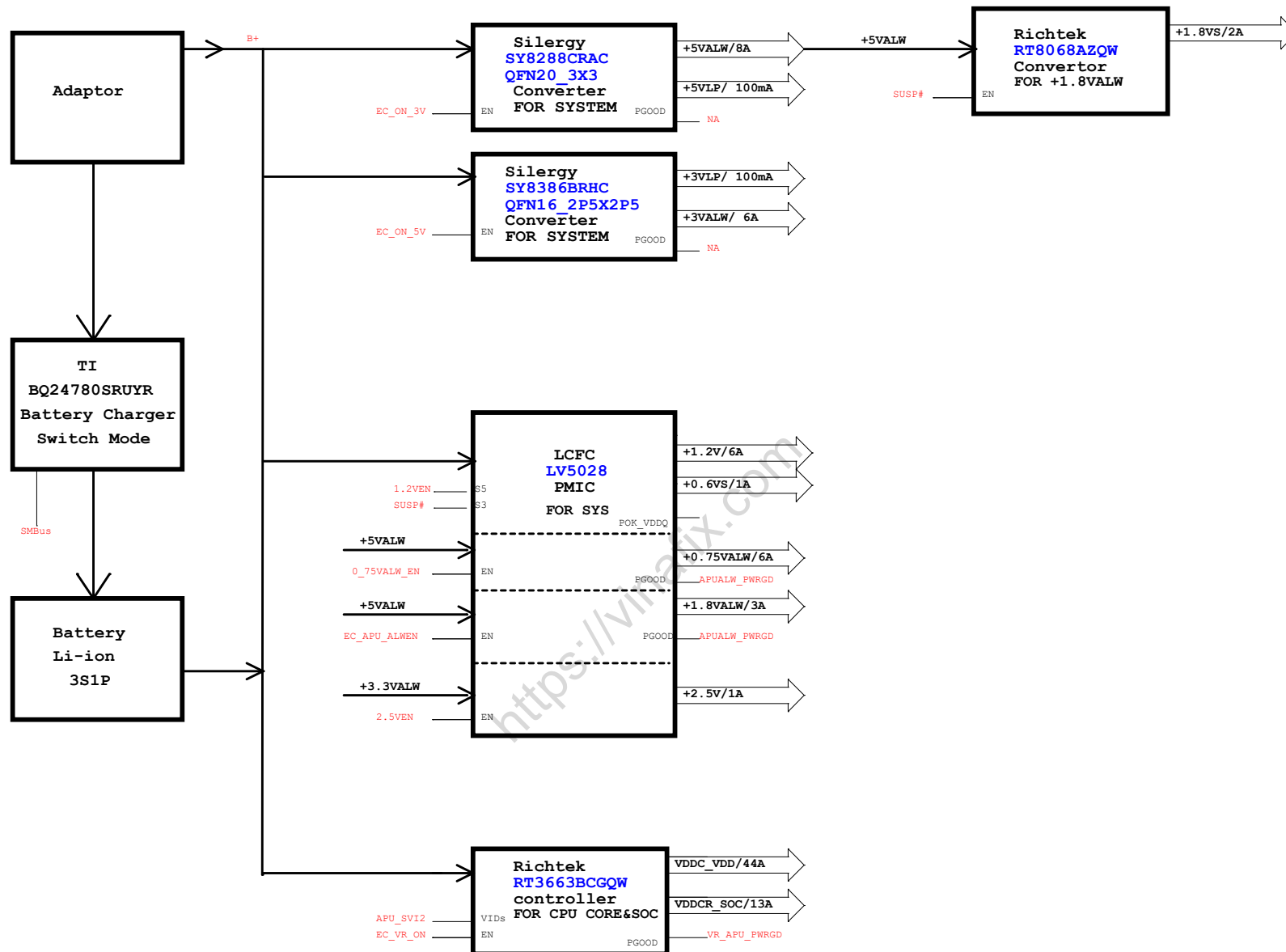
RD228 DDP@
240_0402_1%
SD0000097B7
N

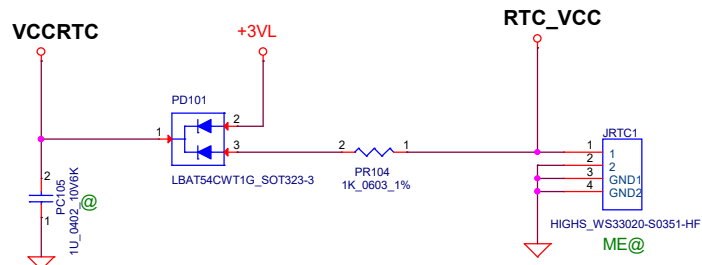
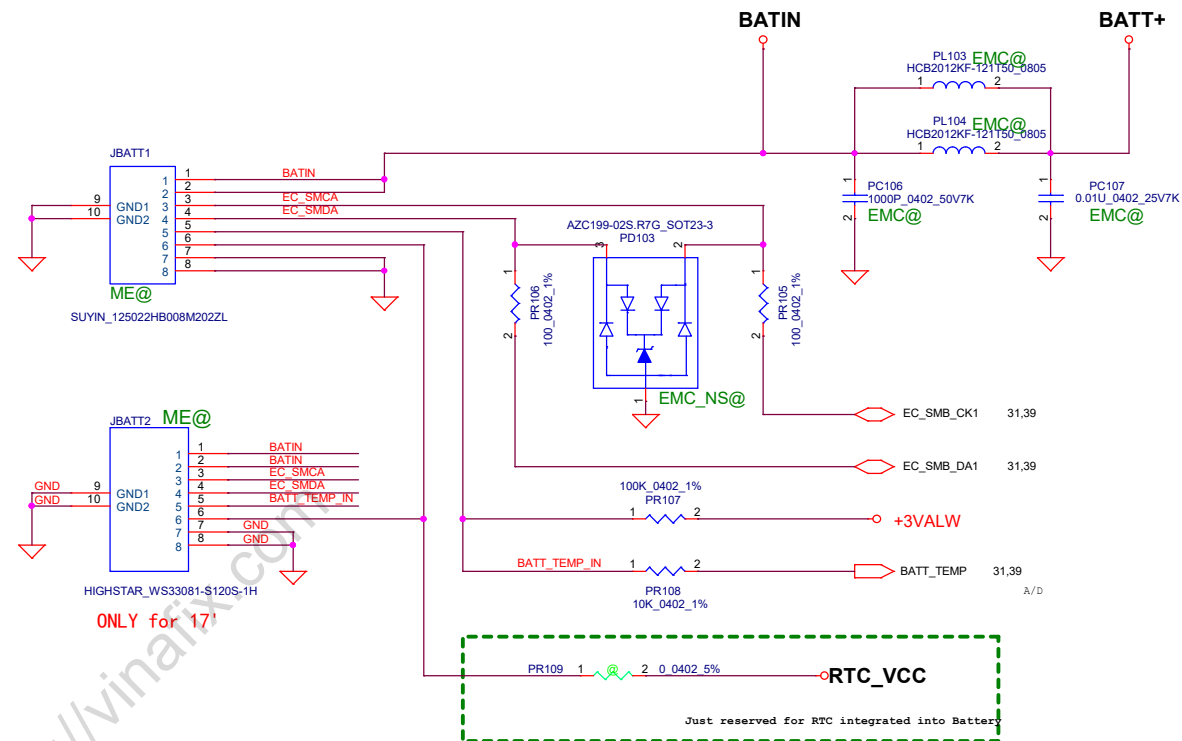
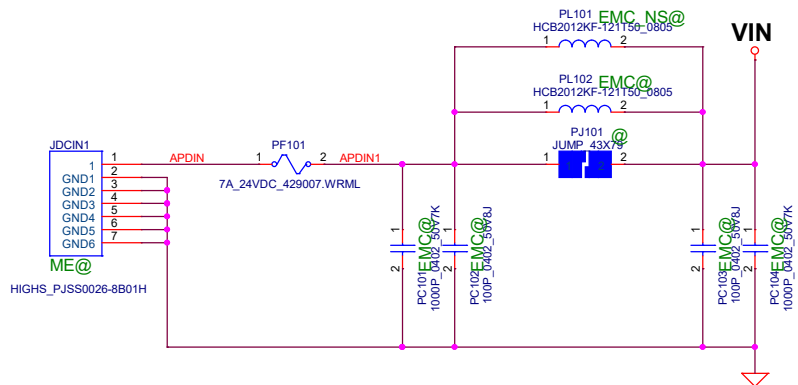
DDP

check ok

<https://vinafix.com>

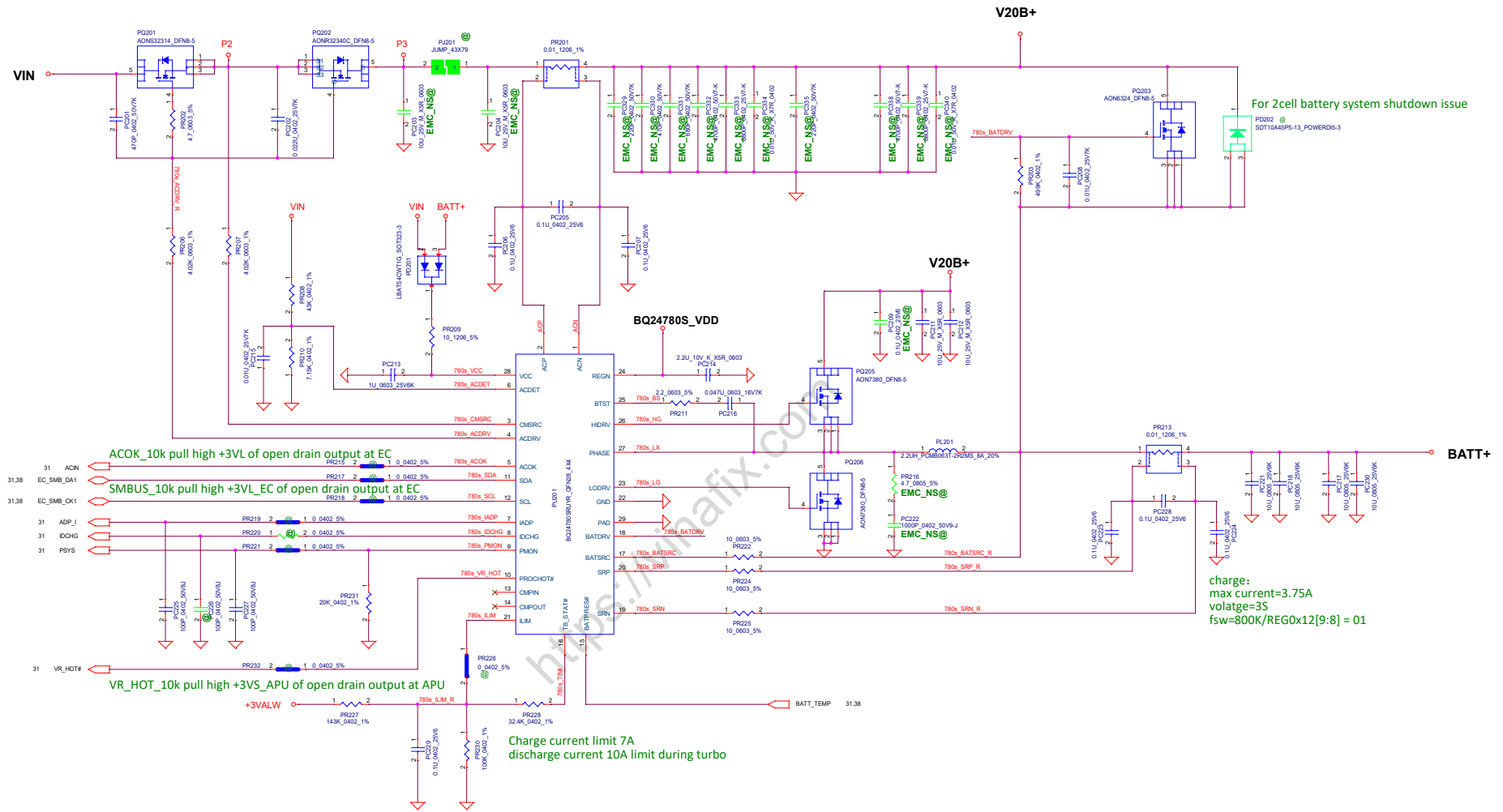
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Issued Date		Deciphered Date		Power sequence Block	
2013/08/15		2013/08/15			
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				Custom	S350 ARE
				Date	Rev
				Sunday, January 19, 2020	1.0
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				36	
				of	
				44	

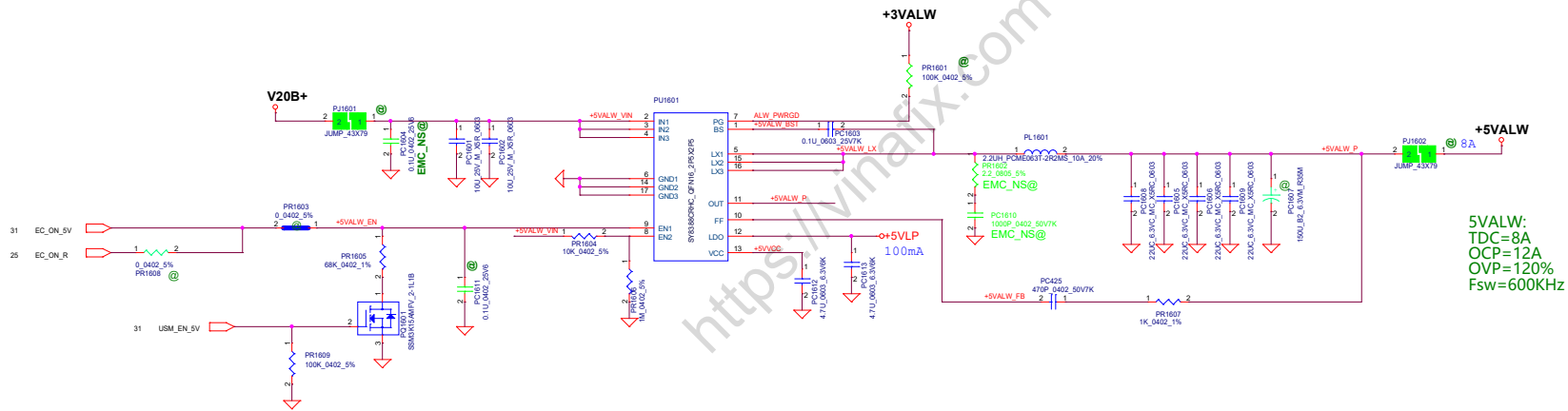
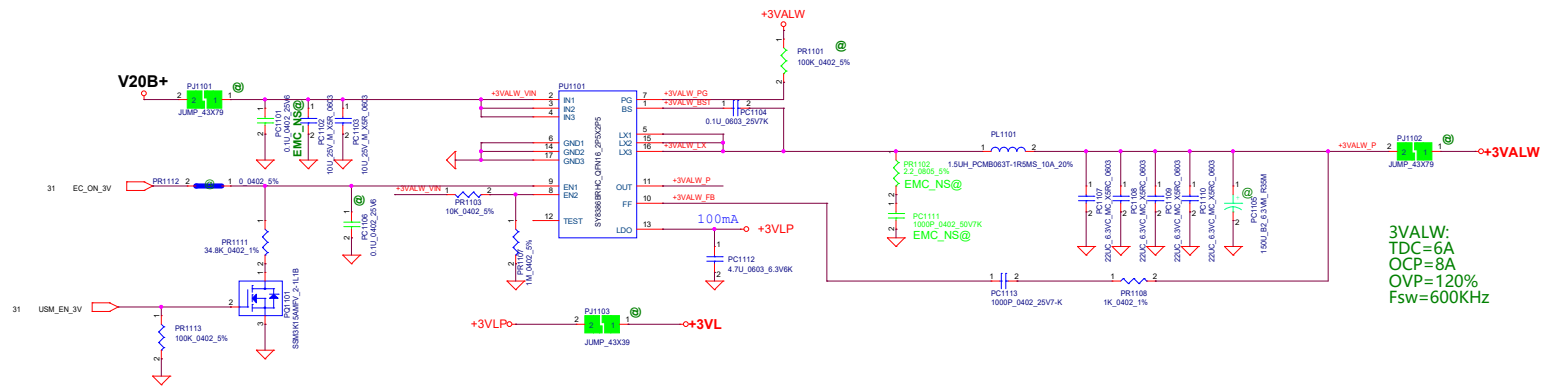


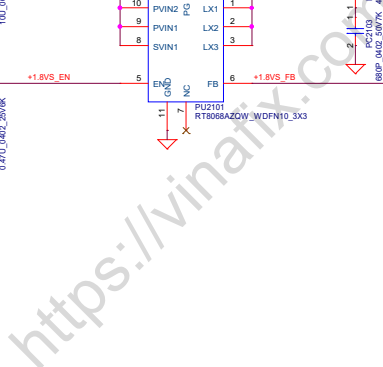


ONLY for 17

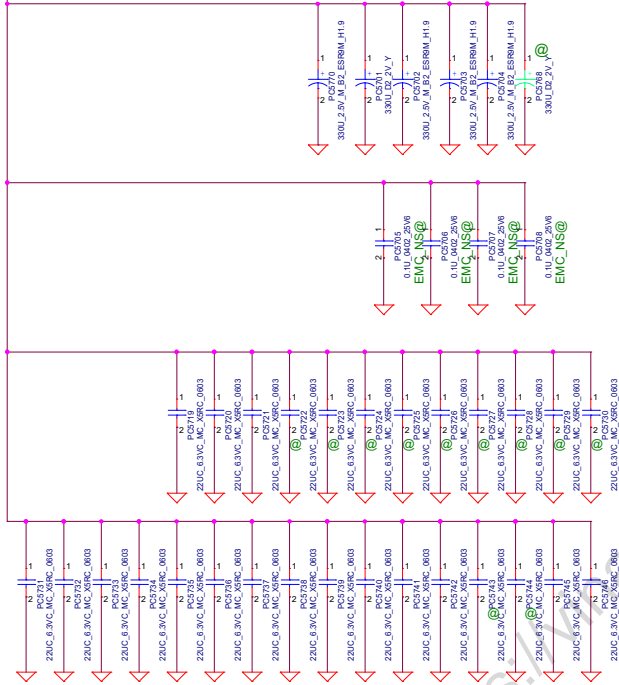
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/15	Deciphered Date	2013/08/15	DCIN / RTC	
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				Rev	1.0



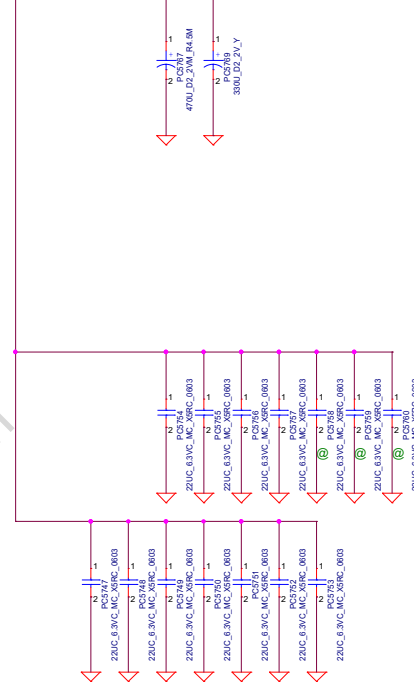


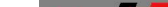


+VDDC_VDD



+VDDCR_SOC



Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		PWR_VDD/SOC decoupling cap	
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